Assessment of Germanane Field Effect Transistors: From Intrinsic Device to CMOS Circuit Performance

by

Yiju Zhao

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Two-dimensional (2D) semiconductors such as transition metal dichalcogenides (TMDs) and black phosphorus (BP) have been in the spotlight for next-generation complementary metal-oxide-semiconductor (CMOS) technology due to their outstanding electronic properties. Recently, germanane (GeH), a hydrogenated germanium monolayer has emerged as a new family of 2D semiconductors. High carrier mobility of GeH as well as promising potential for electronic devices were predicted earlier. However, previous studies were based on a semi-classical model, which cannot properly capture quantum mechanical phenomena generally observed in nanoscale devices. In addition, intrinsic device performance, such as intrinsic delay and switching energy, and circuit-level analyses of GeH field-effect transistors (FETs) are currently absent from the field, the understanding of which will be essential to make use of GeH for future electronic devices. Therefore, in this thesis, a comprehensive study, including material parameterization, device optimization and circuit analysis of GeH FETs will be discussed by means of rigorous self-consistent atomistic quantum transport simulations within a tight-binding approximation.

This thesis covers the following topics: (1) introduction to multi-scale simulations including material parameterization, device simulation and circuit analysis, (2) investigation of transport characteristics and the scaling limit of n-type GeH metal-oxide-semiconductor (MOS) FETs, (3) assessment of GeH MOSFETs for CMOS technology with device optimization, (4) investigation of intrinsic performance of GeH Schottky-barrier (SB) FETs, and (5) discussion of possible future works, such as Ge-GeH heterostructure and multilayer GeH FETs to seek further opportunities. Our results suggest that GeH MOSFET exhibits excellent on-state performance as well as the superior circuit behaviors in terms of energy-delay product. It is also proven that GeH SBFET can be as promising as the MOSFET counterpart despite the performance degradation imposed by the metal-semiconductor junction. Our comprehensive study covering material, device and circuit simulation reveals the significant potential of germanane for the next-generation nanoelectronic devices.

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Chapter 1 Introduction

Complementary metal–oxide–semiconductor (CMOS) technology has been proved to be the most important invention in digital logic circuit. However, the Moore's law was introduced by Gordon Moore in 1965 stating that the computing power will double roughly every two years for constant cost and it has been amazingly held true in the decades since 1970. Nonetheless, conventional fabrication approaches of semiconductor devices are quite close to the fundamental limit of physical scaling. Although it is hard to predict how much further down we can go, we are going to encounter more and more challenges practically and theoretically. New solutions are in demand to help us out of difficulties at nanoscale where the short channel effects become increasingly significant. The revolution in the channel material has emerged as a possible solution to overcome the scaling limit.

It is noted that one of the challenges in scaling devices stems directly from the material, like silicon, which is inherently three-dimensional. Even single-atom-layer silicon is made, it still includes out-of-plane bonds. These dangling bonds require passivation to avoid undesirable interactions, introducing surface roughness that can cause carrier scattering and mobility deterioration [1]. In contrast, there are no such bonds in two-dimensional semiconductors. A single atomic layer is structurally "perfect" and self-passivating, reducing or eliminating short-channel effects. Although many efforts have been put forth to study 2-D material electronic devices in recent years, more works are need. Therefore, I present a study of the device based on a novel 2-D material, germanane.

The principle objectives of the thesis are: (1) to introduce a multi-scale simulation scheme covering material parameterization, device simulation and circuit analysis, (2) to investigate device performance and the scaling limit of n-type GeH metal-oxide-semiconductor (MOS) FETs, (3) to assess GeH MOSFETs for CMOS technology with device optimization, (4) to study the intrinsic performance of GeH Schottky-barrier (SB) FETs, and (5) to discuss possible future works, such as Ge-GeH heterostructure and multilayer GeH FETs for further opportunities.

In the remaining part of this chapter, we will give a brief review of 2-D materials covering the development, state-of-art devices and potential application.

1.1 Two-Dimensional Materials

1.1.1 Development: Beyond Graphene

Two-dimensional (2D) materials have attracted tremendous attention due to their unique properties, such as mechanical flexibility [2], optical transparency [2], [3], and chemical inertness on the surface [4], [5], that the conventional three-dimensional bulk materials can hardly offer inherently. Ever since the first 2D material was obtained by isolating a single layer of graphene from bulk graphite in 2004 [6], many 2D materials have emerged [7]. Despite existing challenges in growth and fabrication, 2D layered materials are regarded as potential key players in diverse fields for electronic, optoelectronic, sensing, and biomedical applications [8]–[13]. Layered materials are also promising for flexible and bendable devices, due to their inherent thinness down to the atomistic scale and the compatibility with plastic substrates [14]. Currently, a common approach to obtain 2D smaples is one of the great challenges toward commercialization. Abundant research samples can be obtained by simple exfoliation. However, the precision and quality requirements of manufacturing demand a more controllable method.

1.1.2 Application: Nanoelectronics

In material science, great interests are shown in related layered materials, such as graphene and silicene. Such materials represent a new generation of semiconductors with potential applications in computer chips and solar cells.

Among many possible applications, 2D materials such as graphene, transition metal dichalcogenides (TMDs), black phosphorus (BP), and silicane, have been explored extensively for electronic device applications for the last decade [15]–[18]. TMDs like molybdenum disulfide (MoS_2) have been studied for low-power switching applications in light of its large band gap and exceptional electrostatic integrity [19]. A microprocessor based on MoS_2 has been developed recently in 2016, demonstrating the feasibility of 2D material-based integrated circuits [20]. Unlike TMDs, black phosphorus has a direct band gap, which can be tunable through its thickness (i.e., by controlling the number of layers) [21]. Due to its high carrier mobility of $\sim 10^3$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ and large ON/OFF current ratio ($I_{ON}/I_{OFF} = 10^5$) [22], BP is considered as a promising candidate for high-performance device applications [23], [24].

1.2 Germanane

Germanane (GeH), a hydrogenated germanium monolayer, has emerged as a new member in the family of 2D materials recently. It is reported that GeH can be synthesized through topotactic deintercalation of CaGe [25]. From calcium germanide, the calcium is removed by de-intercalation with HCl to give a layered solid with the empirical formula GeH. Monolayer germanane has a direct band gap, easily absorbing and emitting light, and is potentially useful for optoelectronics and digital circuit application [26]. First-principle studies here showed its very light effective mass and ultra-high carrier mobility (>18,000 $cm^2/V \cdot s$) [25], [27].

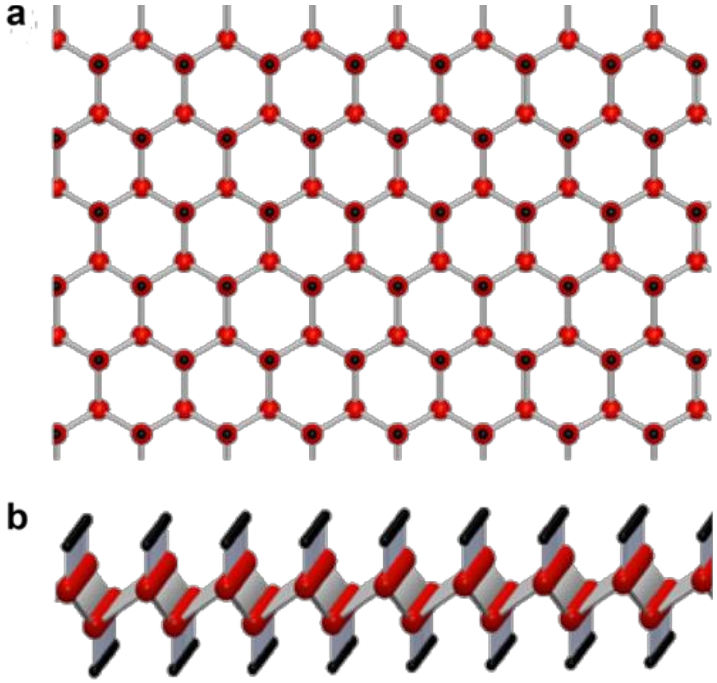

Figure 1.1 Lattice structure of single-layer germanane with Ge atom (red) at the corners of hexagons and H atom (blue) bonded to Ge from (a) top view (b) side view. [28]

1.2.1 Crystal Structure

Germanane is formed as a single layer of germanium (Ge) with hydrogen (H) atoms bonded in the out-of-plane direction on the Ge atoms as shown in Figure 1.1. It has a similar structure to graphene without hydrogen, which is called germanene. However, unlike germanene, GeH is not a perfect 2D material due to the attachment of hydrogen in z-direction, resulting in an open bandgap in GeH, which is critical for logical devices. The unit cell of germanane contains two germanium atoms and two hydrogen atoms as shown in the Figure 1.2 (dashed diamond).

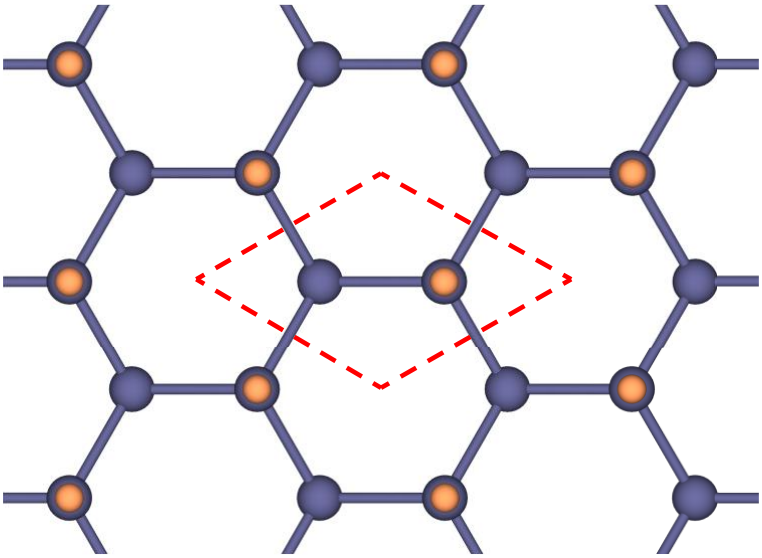

Figure 1.2 Unit cell (red dashed line) of the monolayer germanane.

1.2.2 Band Structure

The band structure of germanane is plotted in Figure 1.3, where the conduction band minimum (CBM) and valence band maximum (VBM) located at the Γ point form a direct band gap of 1.56 eV. The Brillouin zone sampling was done using Monkhorst-Pack approach with a 50 × 50 × 1 mesh.

The calculated band structure exhibits isotropic effective masses around the Γ point. The electron effective mass is 0.07 m_0 and those of heavy hole and light hole are 0.50 m_0 and 0.07 m_0, receptively, where m_0 is free electron mass. The extracted electron and hole effective masses of germanane agree well with reported data from [25], [27]. The effective mass of electrons near CBM is the same as effective mass of light hole and smaller than the heavy hole effective mass. The significantly smaller electron effective mass of germanane indicates higher electron velocity in germanane than that of silicane.

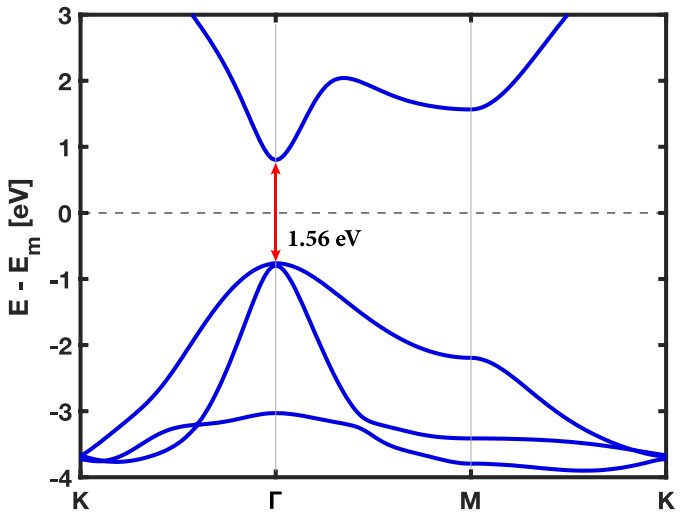

Figure 1.3 Electronic band structure of germanane (GeH) based on density functional theory (DFT).

The contour in Figure 1.4(a) and (b) shows that the lowest conduction band and the highest valence band of germanane are at the Γ valley. The first Brillouin zone has hexagonal shape indicated with the solid line. An isotropic trend is observed in the energy variation around Γ valley for the conduction band, as shown in Figure 1.4 (a). It is noted that the valence band equi-energy contours of both silicane and germanane are highly similar in their topology as evident by their almost identical trend in the hole effective masses.

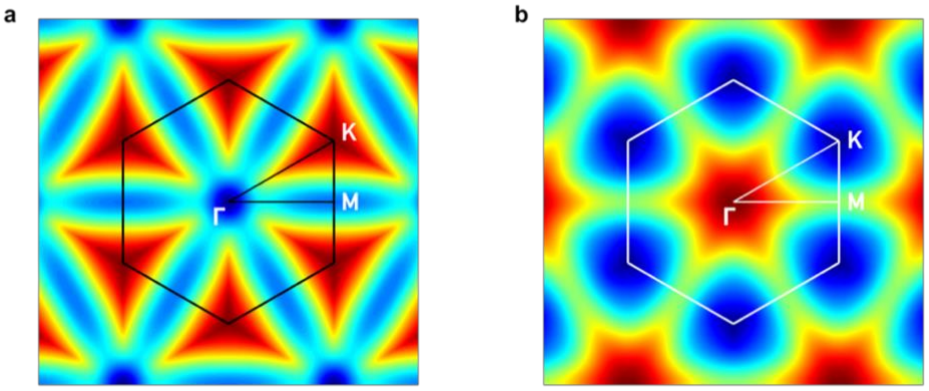

Figure 1.4 Equi-energy contours in k-space (first Brillouin zone has the hexagon shape). (a) CBM and (b) VBM of germanane.

1.2.3 State-of-the-art GeH Electronic Devices

Due to the predicted ultra-high carrier mobility, GeH arrested a great interest for electronic devices. FETs based on GeH as an active channel material have rarely explored although it has great potential for future electronic devices toward various applications. Recently, decent progresses have been made on both experimental and theoretical study of GeH. A research group from Europe have reported on the first field effect transistor fabricated with germanane, highlighting its promising electronic and optoelectronic properties, where a reasonably high field-effect mobility (~150 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and a large ON/OFF current ratio (>10^5) have been measured for GeH field-effect transistors (FETs) as shown in Figure 1.6 [26].

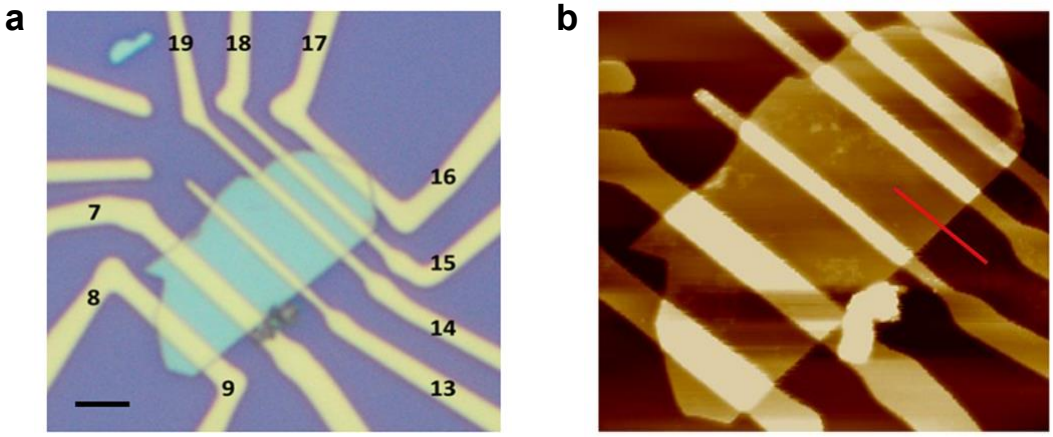

Figure 1.5 (a) Optical image of the GeH flake-based device on top of a Si/SiO2 substrate with Ti/Au electrodes (Scale bar is 3 µm). (b) AFM image of the germanane transistor. [26]

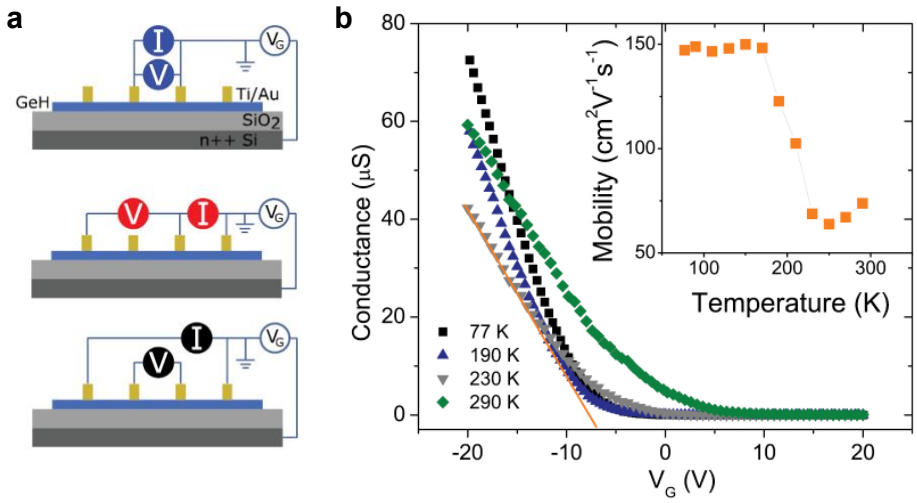

Figure 1.6 (a) Measurement configuration of 2-, 3- and 4-terminal. (b) The 2-terminal conductance is plotted as a function of V_G at different temperatures (77 K, 190 K, 230 K, 290 K). The orange line represents an example of a linear fit for the extraction of hole mobility. The gate voltage was swept from positive to negative values. (Inset) 2-terminal hole mobility extracted from the data plotted in the main panel, shown as a function of temperature. [26]

Chapter 2 Methodology – A Multi-scale Simulation Approach

In conventional MOSFETs simulation, the classical theories are usually adopted for carrier transport calculation, which are based on the Boltzmann transport equation with few or more approximation [29]. As devices scale to the nanometer regime, the classical model that focuses on long channel devices is no longer capable of capturing the property of carrier transport accurately. Devices at nanoscale, operating in a ballistic-transport regime [30], should be modeled and simulated through non-equilibrium Green's function (NEGF) formalism. The performance of GeH FET was estimated previously by semi-classical model [31], but such a simple approach can be significantly limited in predicting the detailed characteristics of germanane device, where quantum-mechanical treatment will be critical to discuss tunneling and scaling. Therefore, in this work, a rigorous self-consistent atomistic quantum transport simulation with the tight-binding method is developed for investigating device performance of GeH FETs.

2.1 Material Parameterization

2.1.1 Density Functional Theory (DFT)

Density functional theory (DFT) is one of the most widely-used and successful quantum mechanical approaches to understand condensed matter physics. In this thesis, DFT are utilized to obtain the band structure of GeH with SIESTA software [32]. Generalized gradient approximations (GGA) is used for computing exchange correlation function, where PBE parameterization was employed for the DFT calculation. Linear combination of atomic orbitals (LCAO) approximation are adopted for constructing basis functions. For a geometry optimization, conjugate-gradients (CG) are used with maximum force tolerance of 10^{-3} eV/Å and energy tolerance of 10^{-4} eV. The band structure of GeH based on DFT calculation is show in Figure 2.1 with red solid lines.

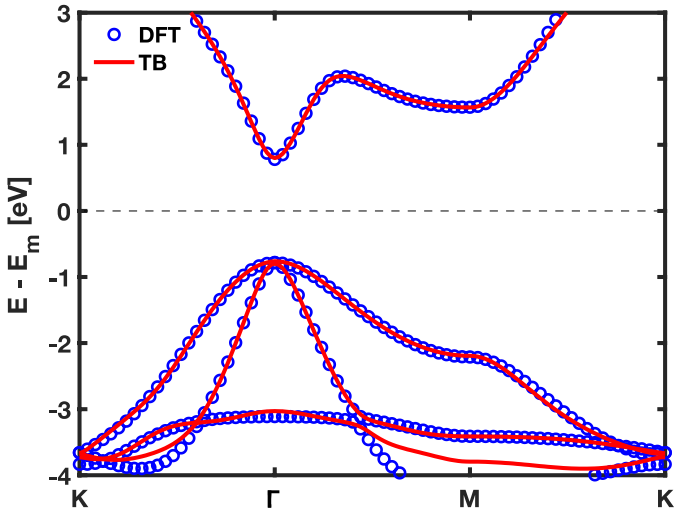

Figure 2.1 Electronic band structure of germanane (GeH) based on density functional theory (blue circles), which is fitted with tight-binding parameters (solid red lines).

2.1.2 Tight-binding Approximation

While ab-initio calculation provides a detailed description of the system, it is a very expensive method in terms of computation. Thus, we would like to use the tight-binding approximation to construct the Hamiltonian matrix for practical device simulation. In the tight-binding method, the eigenstates of the Hamiltonian are written by an atomic-like basis set $\{\varphi_{i\alpha}\}$ and the exact many-body Hamiltonian operator is replaced with a parametrized Hamiltonian matrix. The basis set is atomic-like and has the same symmetry properties as the atomic orbitals. In general, only a small number of basis are used, roughly corresponding to the atomic orbitals in the energy level of interest [33]. The eigenstates of the system are then obtained by solving the characteristic equation.

In this thesis, two-center Slater-Koster approximation [34] was used with second-nearest neighbors to obtain the tight-binding (TB) parameters from the DFT band structure (shown in Figure 2.1 with blue circles). *s* and *p* atomic orbitals were considered for Ge, while only *s* orbital is considered for H. We used an orthonormal basis set. Mean squared error was employed to fit the TB band structure to the DFT one. The resulted TB parameters fit the band structure very accurately near the band edges as shown in Figure 2.1 with solid red lines.

2.2 Device Simulations

The device simulation of GeH FETs are based on a quantum transport simulation, in which the non-equilibrium Green's function (NEGF) is solved self-consistently with electrostatic Poisson's equation [35]. The self-consistent simulation scheme and a three-terminal device configuration with source, drain and gate are shown in the inset of Figure 2.2. *H* is the Hamiltonian matrix for the channel region derived from DFT band structure using tight-binding approximation, *U* describes the self-consistent potential inside the device. Σ_1 and Σ_1 are contact self-energies, describing the electron injection at the channel-contact interfaces. Green's function is calculated for the electron density, which is used in Poisson's equation to solve electrostatic properties. The calculated potential profile is, in turn, used in the NEGF equations to update charge density. These steps will be performed iteratively until a self-consistent result can be achieved.

Periodic boundary condition is applied in the definition of device width, and the charge and the current are calculated by taking the summation of transverse modes in the width direction. Ballistic transport is assumed since the channel length is very short compared with the carrier mean free path and hence the effect of scattering is expected to be minimal. Open boundary conditions are treated with contact self-energies using the Neumann boundary condition.

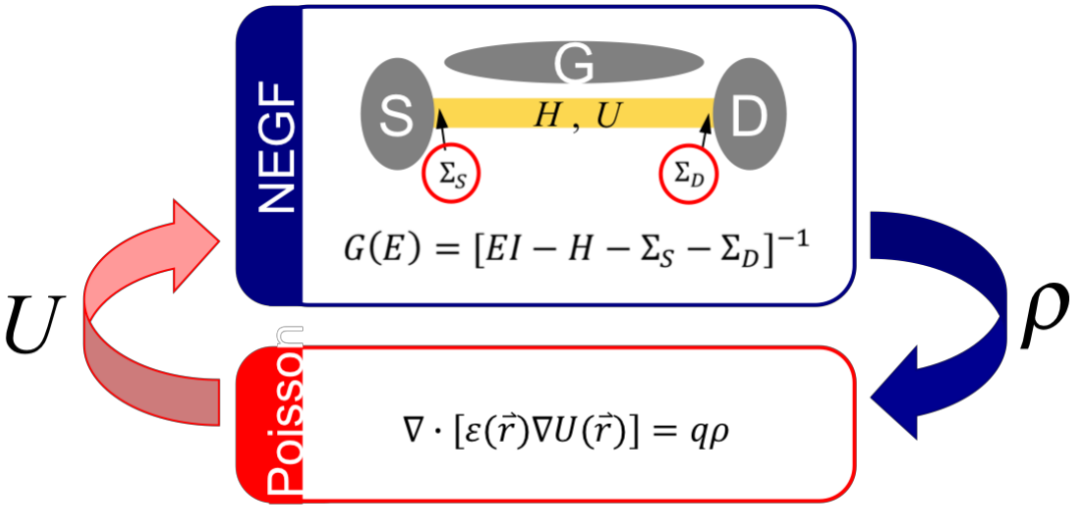

Figure 2.2 The schematic simulation procedure for calculating potential energy (*U*) and carrier density distribution (ρ) self-consistently. (Inset) A 3-terminal device configuration. [36]

2.2.1 Non-equilibrium Green's Function Formalism

A new theory and method of device simulation are needed to help us understand device physics and to better design device at sub-10 nm scale. The theory of quantum mechanics provides an important insight for us to reveal the physics behind the nanoelectronics device. As one of the solid foundations of modern physics, it successfully described novel physical phenomenon at atomic scale, from high energy physics to condensed matter physics. In this thesis, we focus on quantum effects and non-equilibrium, near-ballistic transport in extremely scaled transistors (in contrast to long channel devices). In order to simulate electronic devices at nanoscale where short channel effects become increasingly significant, the non-equilibrium Green's function (NEGF) approach has to be introduced as a powerful tool providing a practical framework to understand those quantum mechanical effects. The NEGF is a technique to solve the non-equilibrium transport equation in the quantum field. The carriers (electrons and holes) behavior within the channel materials constitutes the non-equilibrium distribution of quantum field.

Matrix representation is used in the numerical solutions of NEGF formalism, where the retarded Green's function is defined as follows,

$$G(E) = [EI - H(E) - \Sigma_1 - \Sigma_2]^{-1} \quad 2\text{-}1$$

to describe the system. Discretized real space is indicated by the rows and columns of the matrices. In the equation, H denotes the atomistic-based Hamiltonian deriving from the DFT band structure with tight-binding approximation. Self-energy matrices Σ_1 and Σ_2 describe the contact coupling between the channel region and source/drain. The density spectra of electron and hole are specified by the correlation functions G^n and G^p, which are defined as

$$G^n(E) = G(E)\Sigma^{in}(E)G^\dagger(E) \quad 2\text{-}2$$

$$G^p(E) = G(E)\Sigma^{out}(E)G^\dagger(E) \quad 2\text{-}3$$

After self-consistently solving the NEGF with Poisson equation, the electron density, current density spectrum and local density of state (LDOS) can be evaluated. The broadening function is described as

$$\Gamma_{1,2} = i\left(\Sigma_{1,2} - \Sigma_{1,2}^\dagger\right) \quad 2\text{-}4$$

where $\Sigma_{1,2}^{\dagger}$ is the anti-Hermitian part of "self-energy" matrix. The spectral function is described as

$$A(E) = i\left(G - G^{\dagger}\right) = G^{n} + G^{p} = A_1 + A_2 \tag{2-5}$$

The spectral function *A* represents the matrix version of the density of states per unit energy, and the correlation function G^n is the matrix version of the electron density per unit energy. The electron correlation function is defined as

$$G^{n}(E) = G(\Gamma_1 f_1 + \Gamma_2 f_2)G^{\dagger} \tag{2-6}$$

where f_1 and f_2 are the Fermi function at source and drain, respectively. The current *I* can be defined in the form of

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} I(E)dE \tag{2-7}$$

with $I(E) = T(E)[f_1(E) - f_2(E)]$. Thus, the external current is given by,

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} T(E)\left(f_1(E) - f_2(E)\right)dE \tag{2-8}$$

The transmission can be defined as,

$$T(E) = Tr\left(\Gamma_1 G \Gamma_2 G^{\dagger}\right) \tag{2-9}$$

Charge density also can be determined as,

$$\rho(x) = \int N(E,x)dE \tag{2-10}$$

where

$$N(E,x) = \frac{2G^{n}(E)}{2\pi} = \frac{1}{\pi}\left[G(\Gamma_1 f_1 + \Gamma_2 f_2)G^{\dagger}\right] \tag{2-11}$$

It should be noted that all the theory used in this thesis are based on ballistic transport assumption without considering scatterings due to the relatively short channel length. To see the derivation of the equation above, readers may refer to [35].

2.3 Circuit Analysis

2.3.1 Intrinsic Device Performance

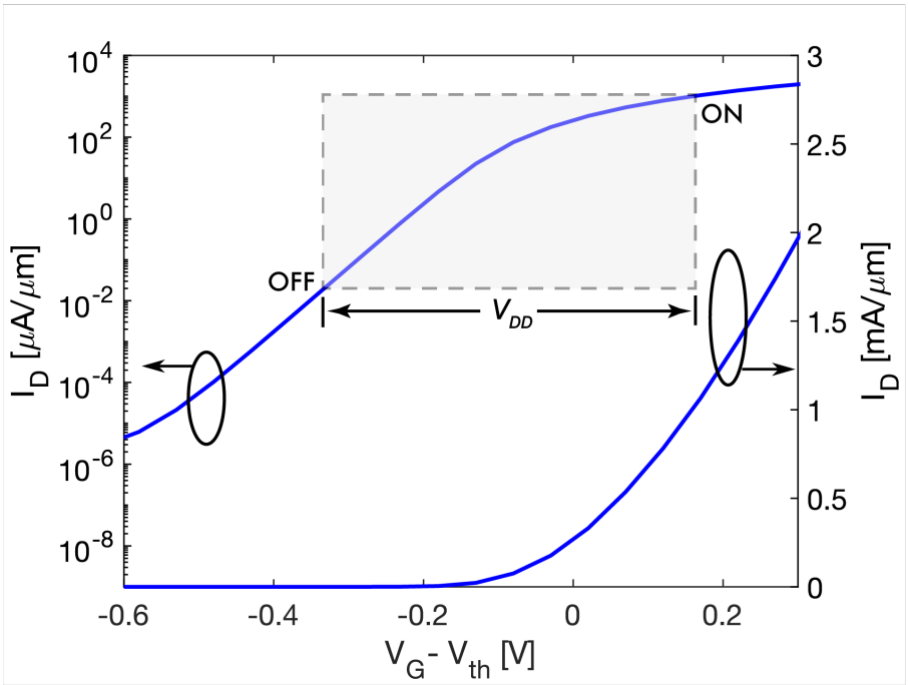

Figure 2.3 A power-supply-voltage (V_{DD}) window defined based on a typical I_D-V_G plot.

In order to better understand the circuit-level behavior, it will be instructive to investigate the intrinsic performance of the individual GeH FET before circuit-level performance is discussed. Intrinsic device delay (τ) is an important performance metric corresponding to the upper limit of switching speed of a transistor. In this thesis, intrinsic delay of the device is calculated as

$$\tau = \frac{Q_{ON} - Q_{OFF}}{I_{ON}} \qquad 2\text{-}12$$

where I_{ON} is ON current, Q_{ON} and Q_{OFF} are the total charges in the channel in the ON state and OFF state, respectively. And ON and OFF states are defined at the edges of the energy window as shown in Figure 2.3. Power delay product (*PDP*) is another intrinsic performance metric indicating energy consumption per switching of a transistor, which is a measure of the dynamic power dissipation, corresponding to charging energy of the MOS capacitor under the voltage bias V_{DD}. In this thesis, *PDP* is evaluated by

$$PDP = (Q_{ON} - Q_{OFF})V_{DD} \qquad 2\text{-}13$$

where parasitic capacitance is ignored. The ON- and OFF- states are defined at the edges of power supply voltage (V_{DD}) window as explained in [37], which will be shifted to find the optimum operational condition for the minimum energy delay product (EDP) [38].

2.3.2 Energy Delay Product (EDP) Optimization

To evaluate the performance of GeH FETs on circuit level, we use normalized propagation delay (τ_{Norm}), normalized energy (E_{Norm}) and normalized energy-delay product (EDP_{Norm}) for the circuit-level figure-of-merits (FOMs), with respect to their capacitance [16], [17]. In this thesis, circuit-level metrics are evaluated by using a simplified CMOS circuit: 15-stage ($L_D = 15$), fan-out one (FO1) inverter chain with an average activity factor ($\alpha = 0.1$) and balanced GeH FETs for NMOS and PMOS. The explicit forms of normalized parameters are defined as below,

$$\tau_{Norm} = \frac{V_{DD}}{I_{ON}} L_D \tag{2-8}$$

Further, total energy E_{Norm} can be written as,

$$\begin{aligned} E_{Norm} &= E_{dyn} + E_{leak} \\ &= \alpha V_{DD}^2 + I_{leak} V_{DD} \tau_{Norm} \\ &= V_{DD}^2 \left(\alpha + L_D \frac{I_{OFF}}{I_{ON}} \right) \end{aligned} \tag{2-9}$$

where E_{dyn} is dynamic energy, E_{leak} is leakage energy and α denote the activity factor. Thus, the energy-delay product (EDP_{Norm}) can be expressed as:

$$\begin{aligned} EDP_{Norm} &= E_{Norm} \cdot \tau_{Norm} \\ &= \frac{L_D V_{DD}^3}{I_{ON}} \left(\alpha + \frac{L_D I_{OFF}}{I_{ON}} \right) \end{aligned} \tag{2-10}$$

Chapter 3 Performance Limit of Germanane FETs

In this chapter, explore the performance limit of monolayer germanane (GeH) field-effect transistors (FETs). We first plotted an electronic band structure of GeH using density functional theory and then tight-binding parameters were extracted. Device characteristics of GeH FETs are investigated using rigorous self-consistent atomistic quantum transport simulations within tight-binding approximations. Our simulation results indicate that GeH FETs can exhibit exceptional on-state device characteristics, such as high ON-state current (I_{ON} >2 mA/μm) and large conductance (g_m ~7 mS/μm) with V_D = 0.5 V due to the very light effective mass of GeH ($0.07m_0$), while maintaining excellent subthreshold swing (SS ~64 mV/dec). We have also performed a scaling study by varying the channel length, and it turned out that GeH FET can be scaled down to ~14-nm channel without facing significant short channel effects but it may suffer from large leakage current at the channel length shorter than 10 nm. Finally, we have benchmarked GeH FET against MoS2 counterpart, exhibiting better suitability of GeH device for high- performance applications compared with MoS_2 transistors.

3.1 Motivation

Nanoelectronics based on two-dimensional (2-D) material has shown great potential in the last decade. 2-D materials like graphene, transition metal dichalcogenides (TMDs) and black phosphorus have proven their utility in various applications such as field-effect transistors (FETs) [1], [2], memory devices [3], and optoelectronics applications [4], [5]. Due to its high carrier mobility and saturation velocity [6], [7], recent graphene research has been mainly focused on high-frequency applications [6]. On the other hand, TMDs like molybdenum disulfide (MoS_2) have been widely explored for low-power switching applications in light of the large band gap and exceptional electrostatic integrity [1].

Recently, germanane (GeH) has emerged as a new family of 2-D materials, which is a single layer of germanium (Ge) with hydrogen (H) atoms attached in the out-of- plane direction [8]. It can be synthesized through topotactic deintercalation of CaGe [8], and first-principle studies showed its very light effective mass and ultra-high carrier mobility (>18,000 $cm^2/V \cdot s$) [8], [9]. However, FETs based on GeH as an active channel material have rarely explored although it has great potential for future electronic devices toward various applications. The performance of GeH FET was estimated previously by semi-classical model [10], but such a simple approach can be significantly limited in predicting the detailed characteristics of germanane device, where quantum-mechanical treatment will be critical to discuss tunneling and scaling. Therefore, in this work, we investigate the performance limit of GeH

FET using rigorous self-consistent atomistic quantum transport simulations. Our simulation results exhibit superior on-state characteristics of GeH FET with excellent switching behaviors. However, due to the very light effective mass, the scaling of GeH FET can be significantly limited as it suffers from large leakage current. We have also benchmarked GeH FET against MoS_2 counterpart, which indicated that GeH FET has clear benefits for high-performance applications compared to a similar device based on MoS_2.

3.2 Simulation Setup

Density functional theory (DFT) calculation [32] was utilized to obtain the band structure of GeH as explained in section 2.1. The unit cell of germanane contains two germanium atoms and two hydrogen atoms as shown in the inset of Figure 3.1(a). The Brillouin zone sampling was done using Monkhorst-Pack approach with a 50 × 50 × 1 mesh. The calculated band structure is shown in Figure 3.1(a), exhibiting isotropic effective masses around Γ point. The electron effective mass is $0.07m_0$ and those of heavy hole and light hole are $0.50m_0$ and $0.07m_0$, receptively, where m_0 is free electron mass, showing good agreements with the reported values in literature [25], [27]. We have corrected the underestimated band gap (E_g) from our DFT calculation to 1.56 eV based on the scissors scheme [12], following the estimated range of E_g = 1.48–1.60 eV in literature [8]. Note that this band gap adjustment does not affect our results at all as we explore only n-type transport behaviors of GeH FET in this study, where the exact value of E_g is out of the picture.

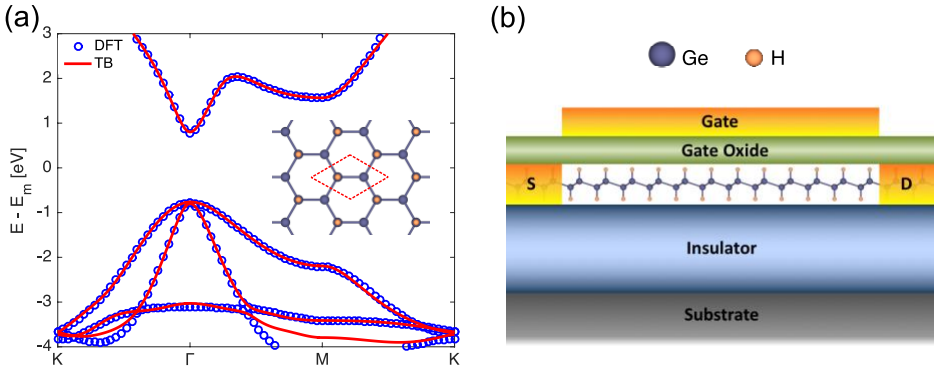

Figure 3.1 (a) Electronic band structure of germanane (GeH) based on density functional theory (blue circles), which is fitted with tight-binding parameters (solid red lines). (Inset) the top view

of germanane lattice with the unit cell represented by red dotted lines. (b) Device structure for the simulated GeH field-effect transistor (GeH FET). [39]

To obtain the tight-binding (TB) parameters from the DFT band structure, two-center Slater-Koster approximation [13] was used with second-nearest neighbors. *s* and *p* atomic orbitals were considered for Ge, while only *s* orbital is taken into account for H. We used an orthonormal basis set. Mean squared error was employed to fit the TB band structure to the DFT one. The resulted TB parameters fit the band structure very accurately near the band edges as shown in Figure 3.1(a). Figure 3.1(b) shows the simulated device structure. Monolayer GeH was used for the channel, and source and drain are n-doped with a doping concentration of 5.5×10^{-12} cm^{-2}. A single-gate device structure is employed through 2.7-nm-thick Al_2O_3 ($\kappa = 9$) for a gate dielectric. The nominal device has a 14-nm channel.

To assess the performance limit of GeH FETs, we have run atomistic quantum transport simulations using the non-equilibrium Green's function (NEGF) method within tight-binding approximations. Transport equations are solved iteratively with Poisson's equation until self-consistency between charge density and electrostatic potential is achieved [35]. Periodic boundary condition is applied for the width of device, and the charge and the current are calculated by taking the summation of transverse modes in the width direction. Ballistic transport is assumed since the channel length is very short and hence the effect of scattering is expected to be minimal. Open boundary conditions are treated with contact self-energies using the Neumann boundary condition. A power supply voltage V_{DD} = 0.5 V (which is smaller than the ITRS requirement) and room temperature are used.

3.3 Device Performance

Figure 3.2(a) shows transfer characteristics of 14-nm-channel monolayer GeH FET (solid lines) at V_D = 0.5 V, plotted both in a logarithmic scale (left axis) and linear scale (right axis). It exhibits excellent switching characteristics with small subthreshold swing (SS ~64 mV/dec) and a large maximum-achievable ON/OFF ratio (~10^{12}) as well as high maximum-achievable on current (I_{on} >2 mA/μm; at V_{on} = 1.2 V and $V_{OFF} = V_{ON} - V_{DD}$). Note that this large I_{on} can be obtained at the sacrifice of I_{OFF}, and we will discuss the detailed relation between I_{on} and I_{on}/I_{off} in Figure 3.4(d). It should be also noted that the current shown in this study is calculated without considering contact resistance to investigate the performance limit of GeH FETs. If the contact resistance is taken into account, current will be reduced to some extent due to the voltage drop across it and hence the lower effective gate and drain voltages across the device, depending on the actual quality of contacts. In spite of its excellent switching

characteristic below the subthreshold voltage, the GeH FET eventually loses its steepness in subthreshold slope at lower gate voltages ($0 < V_G < 0.25$ V in Figure 3.2(a)), unlike other 2D-material FETs. This can be understood by investigating the energy-resolved current spectrum as plotted in Figure 3.2(b) for 14-nm-channel GeH FET at $V_G = 0.25$ V. It reveals that the contribution of tunneling current ($I_{tunneling}$) to the total current ($I_{total} = I_{thermionic} + I_{tunneling}$) is prominent as thermionic current ($I_{thermionic}$) becomes smaller at low gate voltages, resulting in the increase of subthreshold swing. Note that this conspicuous tunneling through 14-nm channel in GeH FET is attributed to its very light effective mass ($0.07m_0$), whereas MoS_2 is known for its sustainability at much shorter channel lengths due to its heavier electron effective mass ($0.55m_0$) [40].

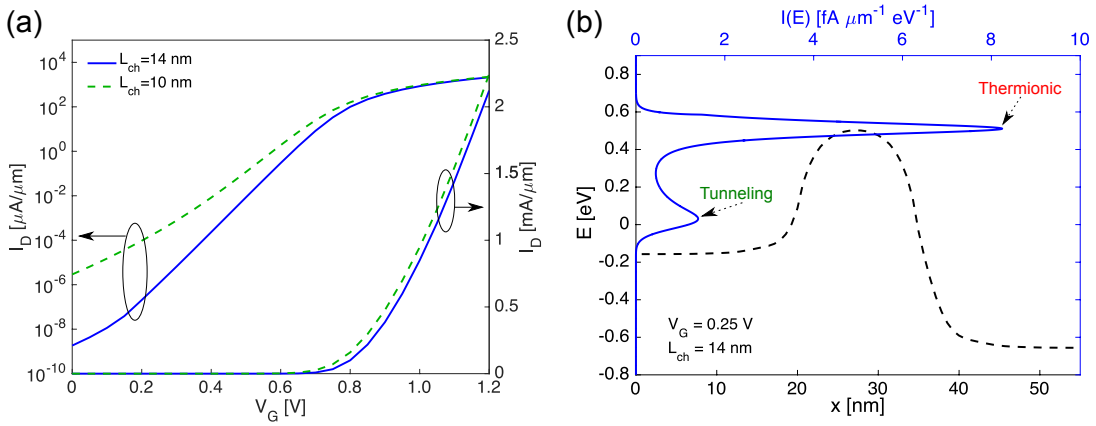

Figure 3.2 (a) Transfer characteristics of monolayer GeH FET with two different channel lengths (L_{ch} = 10 and 14 nm) at V_D = 0.5 V. (b) Energy-resolved current spectrum (blue solid line; top axis) and conduction band (E_c) profile along the device (black dashed line; bottom axis) for 14-nm channel at V_G = 0.25 V and V_D = 0.5 V. [39]

We also simulated 10-nm-channel GeH FET (dashed lines in Figure 3.2(a)) and compared it against 14-nm-channel device. It turned out that the subthreshold swing of 10-nm-channel GeH FET is remarkably greater than 14-nm device due to the significantly larger tunneling current through the thinner barrier. However, both devices having different channel lengths show almost same on current since I_{ON} is dictated mainly by thermionic current at high gate voltages where the effect of tunneling current is infinitesimal.

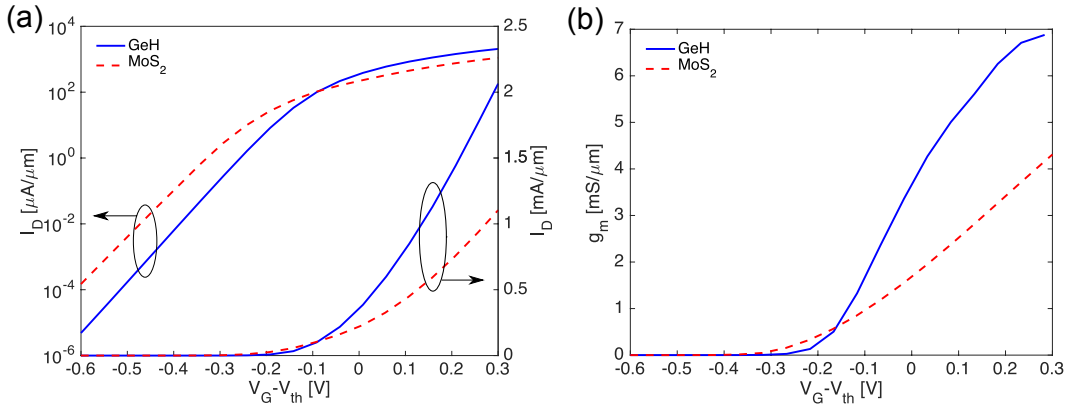

Figure 3.3 (a) I_D vs. V_G–V_{th} for GeH FET and MoS_2 FET both with L_{ch} = 14 nm at V_D = 0.5 V, considering threshold voltage shift. (b) Transconductance g_m vs. V_G–V_{th} for the devices shown in (a). [39]

It will be instructive to benchmark GeH FETs against other similar 2D semiconductor devices. Therefore, here we also simulate 14-nm-channel MoS_2 FET within tight-binding approximation [41], and compare the device characteristics of GeH FET and MoS_2 FET. Figure 3.2(a) and Figure 3.3(b) are I_D and g_m (= $\partial I_D/\partial V_G$) as a function of ($V_G$–$V_{th}$), respectively. While both devices show nearly ideal switching characteristics (SS = 64 mV/dec for GeH; 67.8 mV/dec for MoS_2), GeH FET exhibits significantly better on-state characteristics with 2× larger I_{on} and g_m than MoS_2 FET, which indicates that the gain in carrier velocity is greater than the loss in density of states (DOS) and quantum capacitance (C_Q) through its small effective mass. In principle, higher-κ or thinner dielectric can further boost I_{ON} by increasing oxide capacitance (C_{ox}) at the classical capacitance limit, particularly for the channel material with large effective mass like MoS_2. However, for GeH FET, such improvement can be limited due to extremely small effective mass like MoS_2. However, for GeH FETs, such improvement can be limited due to extremely small effective mass, low DOS and small C_Q. Nonetheless, in order to investigate the detailed effects of larger C_{ox} on device performance, further study will be needed with full self-consistent simulations considering different equivalent oxide thickness since the total gate capacitance is a strong non-linear function of surface potential and charge, which is beyond the scope of this study.

In general, channel length (L_{ch}) is one of the most important device parameters that determine the overall performance of FETs. Moreover, as we have seen in Figure 3.2, device performance of GeH FET can be very susceptible to the actual channel length. Therefore, next, we perform a channel length scaling study of monolayer GeH FETs. Figure 2.4(a) shows SS (= $\partial V_G/\partial \log_{10}(I_D)$) for various channel

lengths from 6 to 22 nm. For the device with $L_{ch} \geq 14$ nm, SS is close to the theoretical limit of 60 mV/dec, but it shows significant increases at sub-10-nm channel lengths, resulting in 175 mV/dec at $L_{ch} = 6$ nm. Similar trend can also be observed for drain-induced barrier lowering (DIBL = $\Delta V/\Delta V_D$) in Figure 3.4(b), which is calculated at $I_{OFF} = 10^{-3}$ μA/μm using $V_D = 0.05$ V and 0.5 V. Thus, it can be concluded from Figure 3.4(a) and Figure 4.4(b) that monolayer GeH FET can be scaled down to ~14 nm without facing significant short-channel effects. We have also investigated how threshold voltage is affected by channel length scaling in Figure 3.4(c). The threshold voltage is ~0.89 V for the channel longer than 14 nm, but it shows V_{th} roll-off at sub-10-nm channel, resulting in $V_{th} = 0.78$ V at $L_{ch} = 6$ nm.

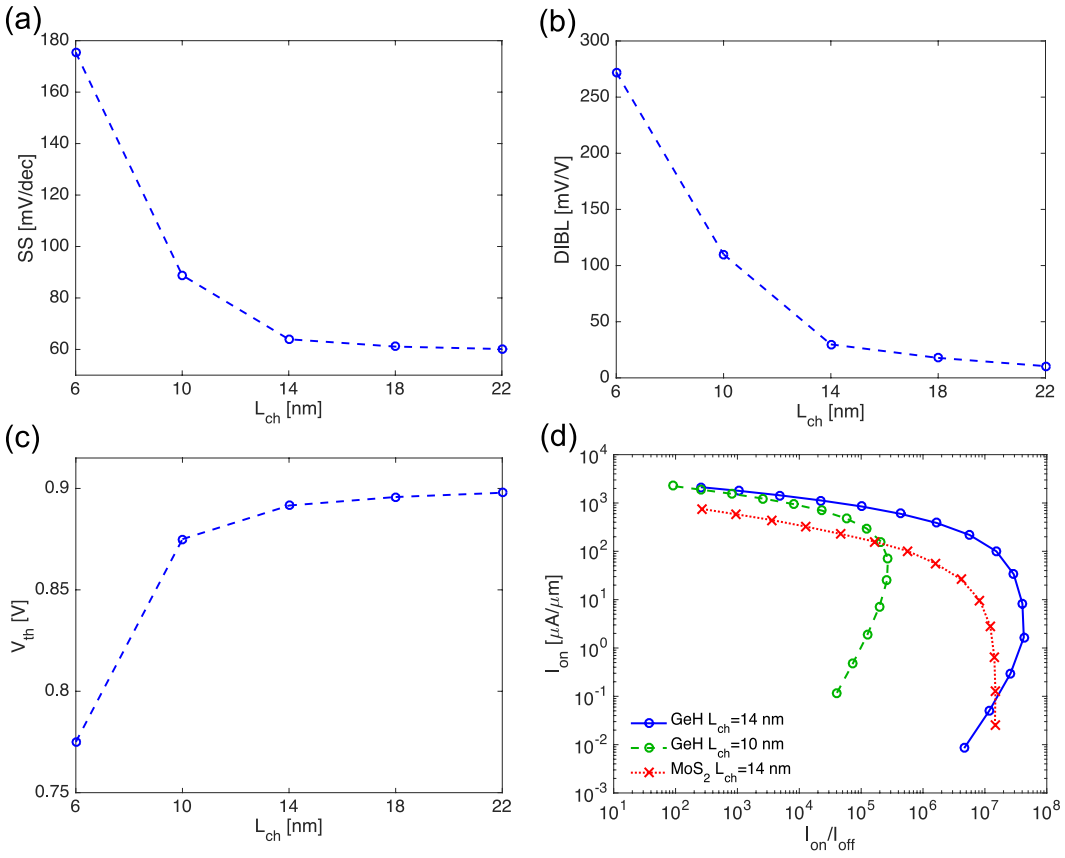

Figure 3.4 (a) Subthreshold swing (SS), (b) drain-induced barrier lowering (DIBL), and (c) threshold voltage (V_{th}) as a function of channel length for the GeH FET. (d) I_{ON} vs. I_{ON}/I_{OFF} for GeH FETs (10-nm and 14-nm channel) and a MoS_2 FET (14-nm channel). [39]

Finally, for comprehensive analyses, we plotted I_{ON} vs. I_{ON}/I_{OFF} for three different devices of GeH FETs (10-nm and 14-nm channel) and a MoS_2 FET (14-nm channel) in Figure 3.4(d), where we have

observed the following points: (1) While both 10-nm and 14-nm-channel GeH FETs can equally provide as high on current as 2 mA/μm, I_{ON}/I_{OFF} is significantly larger with 14-nm-channel device for the same I_{ON}. For example, at a common I_{on} = 100 μA/μm, $I_{ON}/I_{OFF} = 1.53\times10^{7}$ with 14-nm channel, whereas I_{ON}/I_{OFF} of 10-nm channel device is 2.42×10^{5}. (2) Although both GeH FET and MoS_2 FET with the same 14-nm channel can provide as large ON-OFF current ratio as $I_{ON}/I_{OFF} > 10^{7}$, I_{ON} of GeH FET can be significantly higher than that of MoS_2 FET for the same I_{ON}/I_{OFF}. For instance, at a common $I_{ON}/I_{OFF} = 10^{5}$, on current is 850 μA/μm and 183 μA/μm for GeH FET and MoS_2 FET, respectively. (3) In addition, we notice a unique shape of the curves in the I_{ON} vs. I_{ON}/I_{OFF} plots for GeH FETs, which can be distinguished from those of other 2D-material FETs such as MoS_2 (dotted line with crosses in Figure 3.4(d)) and black phosphorus [42]. While other materials show the monotonic increase of $I_{ON}/I_{OFF}$by sacrificing I_{ON}, GeH FETs exhibit non-monotonic behaviors due to the tunneling current at low gate voltages as discussed earlier.

3.4 Summary

We explored the performance limit of monolayer GeH FETs using self-consistent atomistic quantum transport simulations. GeH FET exhibits superior on-state device performance such as high I_{ON} (>2 mA/μm) and large g_m (~7 mS/μm), due to its very light effective mass, as well as excellent switching characteristics (SS ~64 mV/dec). Our scaling study revealed that ~14 nm will be suitable for the channel length of GeH FET as it may suffer from significant short channel effects if the channel length becomes less than 10 nm. We have also benchmarked GeH FET against MoS_2 device, which suggested that GeH has clear benefits for high-performance device applications over MoS_2.

Chapter 4 Assessment of GeH FETs for CMOS Technology

In this chapter, we provide a comprehensive study including material parameterization, device simulation, and circuit analyses demonstrates significant potential of GeH FETs for 2D-material CMOS circuit applications. We assess GeH-based CMOS technology through rigorous quantum transport simulations of both n-type GeH FET (NMOS) and p-type counterpart (PMOS). Using self-consistent atomistic quantum transport simulations, the device characteristics of n-type and p-type germanane (GeH) field-effect transistors (FETs) are evaluated. While both devices exhibit near-identical OFF-state characteristics, n-type GeH FET shows ~40% larger on current than the p-type counterpart, resulting in faster switching speed and lower power-delay product. Our benchmark of GeH FETs against similar devices based on 2D materials reveals that GeH outperforms MoS_2 and black phosphorus in terms of energy-delay product (EDP). In addition, the performance of GeH-based CMOS circuit is analyzed using an inverter chain. By engineering power supply voltage and threshold voltage simultaneously, we find the optimal operating condition of GeH FETs, minimizing EDP in the CMOS circuit.

4.1 Background

Two-dimensional (2D) semiconductors such as transition metal dichalcogenides and black phosphorus have been in the spotlight for electronic device components of next-generation complementary metal-oxide-semiconductor (CMOS) technology due to their intriguing electrical and mechanical properties [9], [22]. For instance, a microprocessor based on molybdenum disulfide (MoS_2) has been demonstrated, exhibiting significant potential of 2D semiconductors for integrated circuits [20]. Recently, a new family of 2D materials based on group-IV such as germanane (GeH) and silicane has emerged [25], [43], [44]. GeH is a light-effective-mass material ($m_e^* < 0.1m_0$), and an exceptionally high carrier mobility (>18,000 $cm^2/V \cdot s$) is theoretically predicted [25], while measured mobility of GeH field-effect transistor (FET) is still limited to much lower values (30 $cm^2/V \cdot s$) [26]. In addition, promising characteristics of GeH FETs have been predicted for high-performance applications [27], [31], [39]. Although n-type GeH FETs have been carefully investigated based on atomistic quantum transport simulations [39], in-depth understanding of p-type GeH device is currently absent from the field. Notably, GeH has heavy holes and light holes, which cannot be captured with semi-classical models [31]. Moreover, to assess the GeH-based CMOS circuit performance, the characteristics of both n-type and p-type transistors should be accurately evaluated using rigorous atomistic quantum transport simulations.

In the following section, n-type and p-type GeH FETs are investigated individually using self-consistent atomistic quantum transport simulation with tight-binding (TB) parameters extracted from density functional theory (DFT) bands. Furthermore, intrinsic device performance metrics such as intrinsic delay and power-delay product are evaluated and compared against other similar 2D material devices. Finally, circuit-level analyses are conducted to optimize the operating condition of GeH FETs by engineering power supply voltage (V_{DD}) and threshold voltage.

4.2 Simulation Method

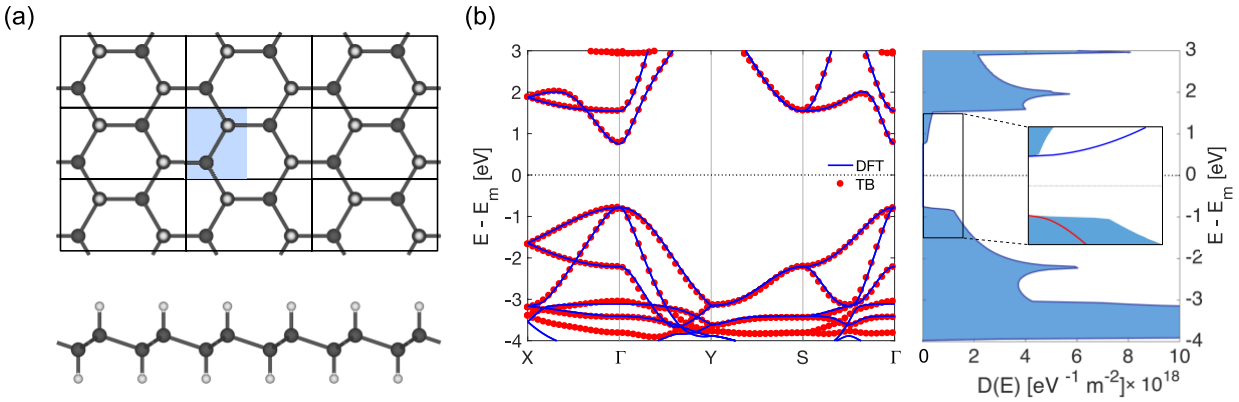

Figure 4.1 (a) Top view (top panel) and side view (bottom panel) of GeH supercells chosen for NEGF simulation. Each supercell (black solid box) consists of two unit cells (blue shaded box). (b) (Left panel) Electronic band structure of the GeH supercell from DFT calculation (blue lines). Tight-binding (TB) bands are also shown (red dots), exhibiting an excellent matching with the DFT bands. (Right panel) Density of states (DOS) of GeH, showing the significant difference of DOS in the conduction band (E_c) and the valence band (E_v). (Inset) A zoom-in plot of DOS near the band edges. The blue and red solid line in the inset represent the group velocity of electrons and holes, respectively. [38]

Electronic properties of GeH are described by TB parameters, which have been achieved through numerical fitting of the DFT band structure [39]. Transport properties are simulated based on the non-equilibrium Green's function (NEGF) method within a TB approximation, while self-consistent electrostatic potential is achieved by solving the Poisson's equation alongside the transport equation [35]. The following parameters are chosen for a nominal device: Monolayer GeH is used for the active material of the device. Channel length (L_{ch}) is 15 nm and source/drain extensions are 20 nm. 3.85-nm-thick Al_2O_3 (κ = 9) are used with a single-gate geometry. Source/drain doping concentration is

8.25×10^{12} cm^{-2} for the n-type device, whereas a higher doping concentration of 1.65×10^{13} cm^{-2} is used for p-type GeH considering its larger density of states (DOS). Ballistic transport is assumed due to the relatively short channel length considered in this study. A supercell, consisting of two unit cells [Figure 4.1(a)], is chosen to construct a Hamiltonian matrix (H) for the NEGF simulation. The left panel of Figure 4.1(b) presents the band structure of the GeH supercell based on both DFT and TB, exhibiting the accurate description of electronic states with TB parameters, which is inherently impossible in semi-classical models. The right panel of Figure 4.1(b) shows the DOS of GeH, which reveals that the DOS of near the valance band edge (E_v) is ~6× larger than that near the conduction band edge (E_c).

4.3 Transfer Characteristics of n and p-type GeH FETs

Figure 4.2(a) shows the transfer characteristics of n-type and p-type GeH FETs in both a logarithmic scale (left axis) and a linear scale (right axis). While both devices exhibit near-ideal switching characteristic (SS ~68 mV/dec), it is observed that NMOS has ~40% larger on current than PMOS. To understand this, energy-resolved current spectrum (solid line; top axis) is plotted for the n-type and p-type GeH FET in Figure 4.2(b) and Figure 5.2(c), respectively, along with potential profile (dashed line; bottom axis) in the on state ($|V_G|$ = 1.1 V). It is observed that NMOS has a wider current spectrum compared to PMOS due to the lower potential barrier at the same $|V_G|$. This is attributed mainly to the smaller DOS of n-type GeH, making the modulation of potential barrier by the gate easier. Although charge density in NMOS is limited by its small DOS, NMOS exhibits larger I_{ON} than PMOS due to fact that the gain in the carrier velocity overcomes the loss in charge density [39]. Notably, higher carrier velocity in NMOS is the result of the contributions of both large injection velocity (as shown in the inset of the right panel of Figure 4.1(b)) and large energy window for current flow as explained above. To evaluate both on and OFF states simultaneously, we plot I_{ON} vs. I_{ON}/I_{OFF} in Figure 4.2(d) by shifting the V_{DD} window [dotted lines in Figure 4.2(a)], which exhibits that NMOS outperforms PMOS device. For the same I_{ON} = 500 μA/μm, NMOS shows $I_{ON}/I_{OFF} = 1.2\times10^5$, which is larger than that of PMOS by ~1 order of magnitude.

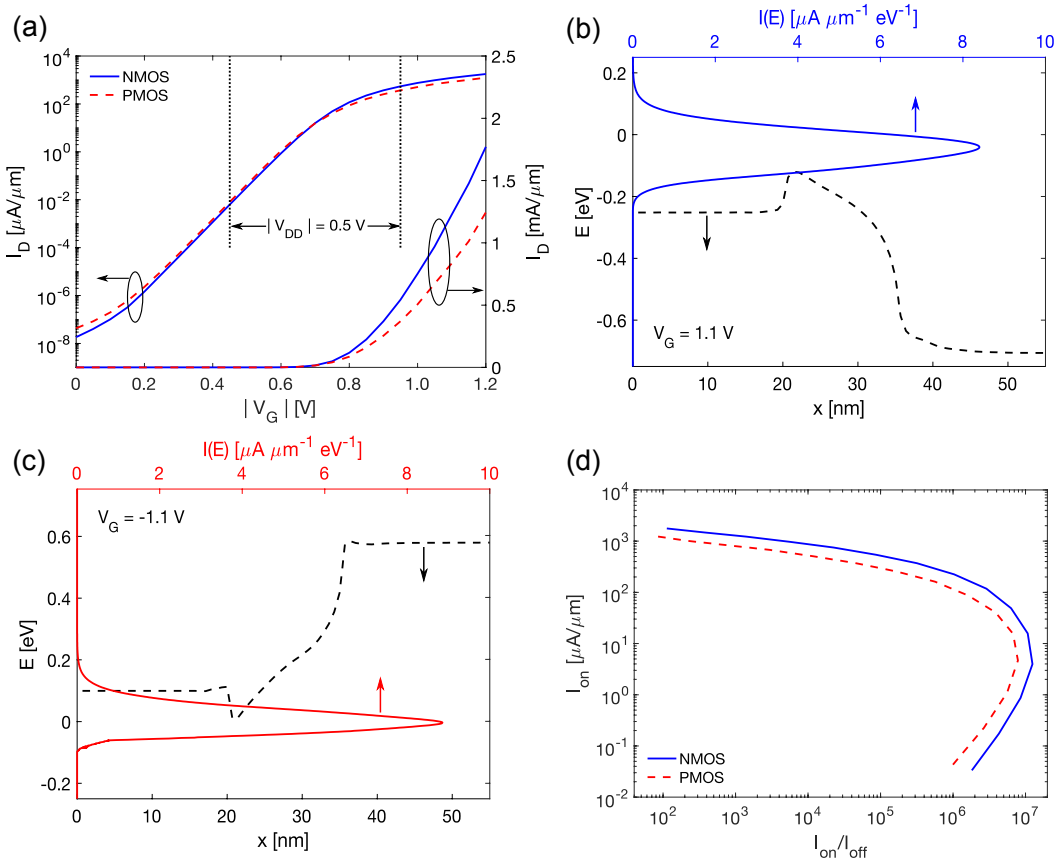

Figure 4.2 Transfer characteristics of n-type and p-type monolayer GeH FETs. (a) I_D–$|V_G|$ curves at $|V_D|$ = 0.5 V. V_G and V_D are positive (negative) for the n-type (p-type) transistor. (b) and (c) are energy-resolved current spectrum of the n-type (blue solid line; top axis) and the p-type (red solid line; top axis) GeH FET, respectively, at $|V_G|$ = 1.1 V and $|V_D|$ = 0.5 V. E_c and E_v are also shown in (b) and (c), respectively, along the device (black dashed line; bottom axis). (d) I_{on} vs. I_{on}/I_{off} plotted by shifting the position of the V_{DD} window shown in (a). ON (OFF) state is defined at the right (left) boundary of the V_{DD} window. [38]

4.4 Intrinsic Device Performance

It will be instructive to investigate the intrinsic performance of the individual GeH FET before circuit-level performance is discussed. Here we evaluate two important device performance metrics: intrinsic delay (τ) and power-delay product (PDP), which correspond to the intrinsic limitation of switching speed and the dynamic power dissipation, respectively. Utilizing the simulation results, the intrinsic

device characteristics are evaluated as $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$ and PDP = $(Q_{ON} - Q_{OFF})V_{DD}$, illustrated in methodology section. Figure 4.3(a) shows τ vs. I_{ON}/I_{OFF} for NMOS and PMOS at a constant $|V_{DD}| = 0.5$ V. Switching speed, or inverse of the delay, of both devices monotonically increases as the V_{DD} window shifts from the subthreshold to the super-threshold region. It should be noted that switching speed of NMOS is faster than PMOS at high gate voltages, which is mainly due to the larger on current of NMOS as shown in Figure 4.2(a). PDP vs. I_{ON}/I_{OFF} is shown for NMOS and PMOS in Figure 4.3(b), where switching energy increases commonly for both NMOS and PMOS as the device switches at higher gate voltages. It was observed that NMOS needs less energy to be switched. It should be noted that the non-monotonic behaviors observed at large delay and small PDP in Figure 4.3(a) and (b) are attributed to the tunneling component existing at low gate voltages as shown in Figure 4.2(a), which is consistent with a previous report [39]. We also plotted PDP-delay trade-off curves in Figure 4.3(c), which manifests the inverse relation of switching energy and delay. Energy-delay product (EDP) of transistor is a figure of merit for the intrinsic device performance. The optimal point can be determined at τ = 46.3 fs and PDP = 11.7 aJ/μm for NMOS and at τ = 46.1 fs and PDP = 28.7 aJ/μm for PMOS, where a product of PDP and τ becomes minimum for each device. These optimal points of GeH-based NMOS and PMOS are plotted in Figure 4.3(d), in which other similar 2D semiconductor devices, namely MoS_2 FETs [45] and black phosphorus (BP) FETs [46], are also included for comparison along with the ITRS 2024 requirement [47]. In general, 2D-material FETs have fast switching speed and low switching energy as compared to the ITRS 2024 requirement. Among them, GeH FETs exhibit the best performance with the lowest EDP ($< 2\times10^{-30}$ J·s/μm).

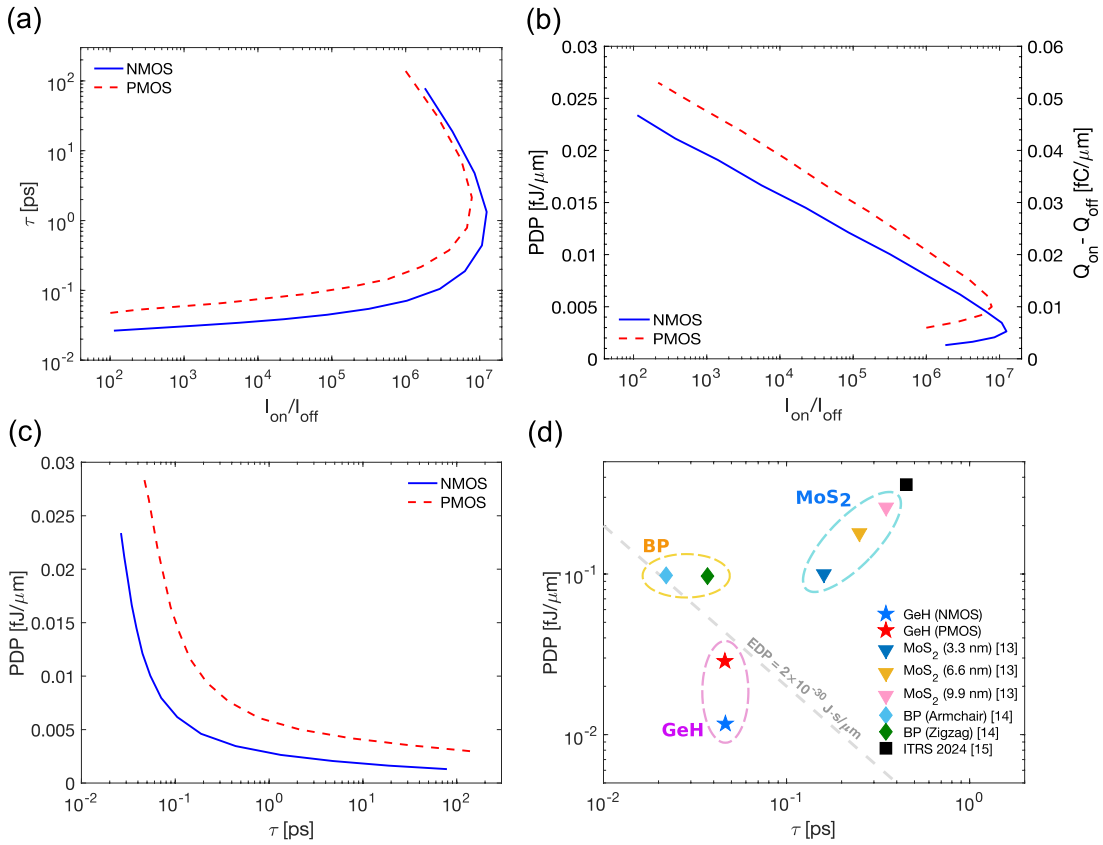

Figure 4.3 Intrinsic device performance metrics. (a) Intrinsic delay (τ), (b) power-delay product (PDP; left axis) and $Q_{on} - Q_{off}$ (right axis) as a function of I_{on}/I_{off}. (c) PDP–τ relations. (d) Benchmark of GeH FETs against similar FETs based on MoS_2 and black phosphorus (BP). ITRS 2024 requirement (black square) is also shown. The gray dashed guideline represents EDP = 2×10^{-30} J·s/μm. [38]

4.5 Energy-delay-product (EDP) Optimization

Next, we discuss the circuit-level performance of GeH FETs. We use normalized propagation delay (τ_{Norm}), normalized energy (E_{Norm}) and normalized energy-delay product ($\mathrm{EDP}_{\mathrm{Norm}}$) for the circuit-level figure-of-merits (FOMs), following the method used for a similar study [48], [49]. Those circuit-level metrics are evaluated by using a simplified CMOS circuit: 15-stage ($L_d = 15$), fan-out one (FO1) inverter chain with an average activity factor ($\alpha = 0.1$) and balanced GeH FETs for NMOS and PMOS. First, we plot the normalized circuit-level FOMs as a function of I_{off} by changing the position of the V_{DD} window for a fixed V_{DD}. While τ_{Norm} can be decreased by increasing I_{off} (*i.e.*, reducing threshold voltage), it comes with the cost of increasing E_{Norm} since the normalized leakage energy becomes

dominant in the super-threshold region as shown in Figure 4.4(a). Therefore, by considering τ_{Norm} and E_{Norm} simultaneously, the optimum point can be determined. Figure 4.4(b) presents the normalized energy-delay product as a function of I_{OFF}. For V_{DD} = 0.5 V, the minimum $\mathrm{EDP}_{\mathrm{Norm}}$ = 0.17 J·s/(F^2/mm), which is a 47% improvement as compared to the maximum value observed at I_{off} = 10^{-2} μA/μm. Notably, the minimum $\mathrm{EDP}_{\mathrm{Norm}}$ can be further reduced by engineering power supply voltage. If V_{DD} = 0.4 V is used, $\mathrm{EDP}_{\mathrm{Norm}}$ decreases by 13% compared to that with V_{DD} = 0.5 V. This indicates that smaller V_{DD} should be taken into account for the global optimization of operating condition of GeH FETs for CMOS circuits. Therefore, next we investigate the effect of V_{DD}. Figure 4.4 (c)-(e) show τ_{Norm}, E_{Norm} and $\mathrm{EDP}_{\mathrm{Norm}}$ as a function of V_{DD}, where the mid-point of V_{DD} window [V_m = (V_{ON} + V_{OFF}) / 2] is fixed at 0.7 V.

4.6 Summary

In this chapter, monolayer GeH NMOS and PMOS are evaluated for CMOS technology, based on self-consistent atomistic quantum transport simulations. While both NMOS and PMOS have excellent switching characteristics (SS ~68 mV/dec), n-type GeH exhibits ~40% better on-state performance due to its high carrier velocity, compared to the p-type counterpart. We also calculated intrinsic delay and switching energy of GeH FETs and compared with similar 2D material FETs, exhibiting clear benefits of GeH over MoS_2 and BP in terms of energy-delay product. Furthermore, by engineering V_{DD} and threshold voltage, we identified the optimal operating condition of GeH FETs to minimize energy-delay product in CMOS circuits. Our comprehensive study covering material, device and circuit suggests that germanane can be a significant contender for electronic devices of next-generation CMOS technology.

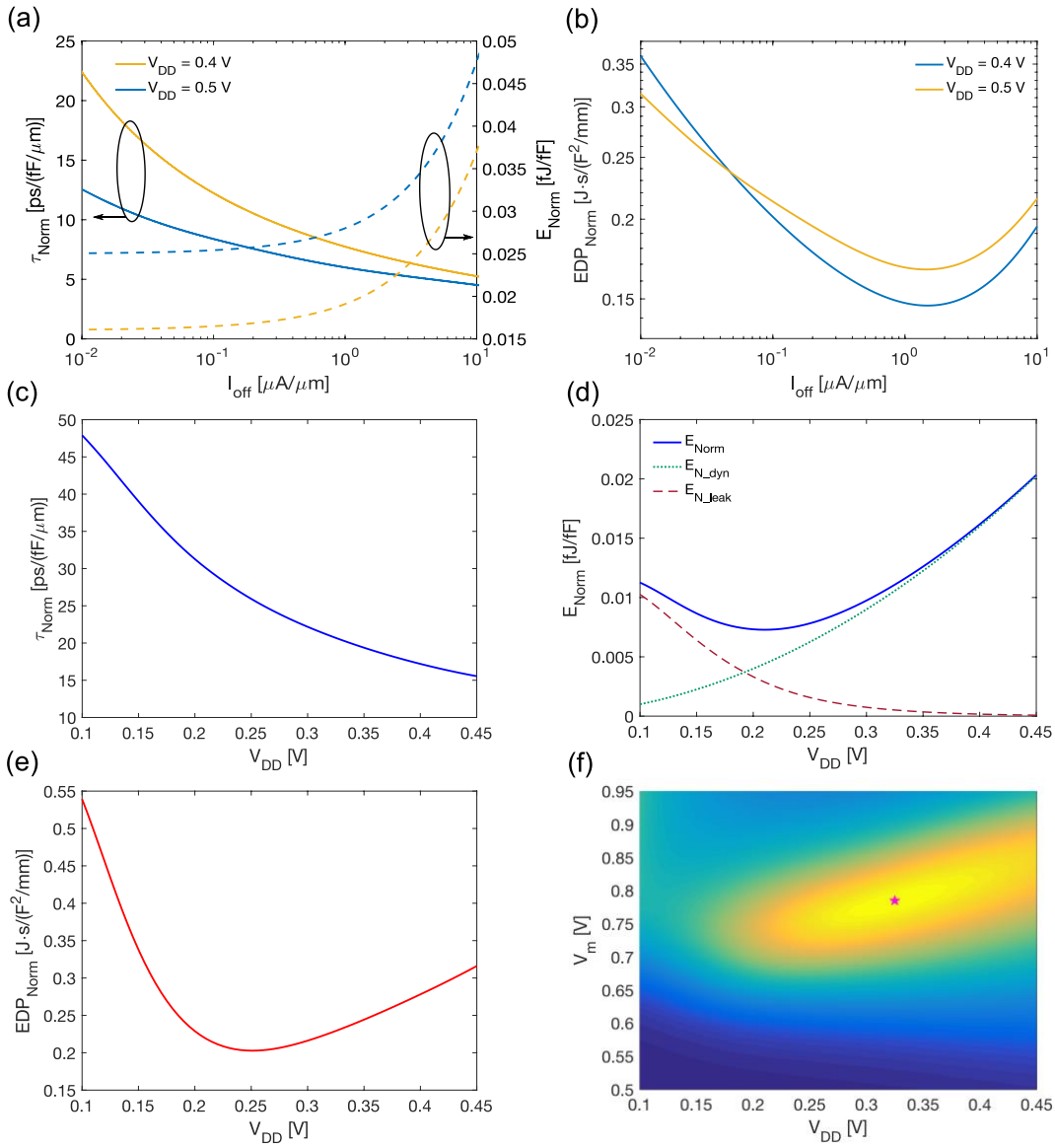

Figure 4.4 Optimization of circuit-level figure-of-merits. (a) Normalized propagation delay (τ_{Norm}) and normalized energy (E_{Norm}), and (b) normalized energy-delay product (EDP_{Norm}) as a function of I_{off} at V_{DD} = 0.4 V and 0.5 V. (c) τ_{Norm}, (d) normalized total energy (solid line), dynamic energy (dotted line) and leakage energy (dashed line), and (e) EDP_{Norm} as a function of V_{DD} with the mid-point of V_{DD} window fixed at V_m = 0.7 V. (f) Color map of 1/EDP_{Norm} for various V_{DD} and V_m. [38]

Chapter 5 Germanane Schottky-barrier FETs

5.1 Motivation

Recently, germanane (GeH), a hydrogenated germanium monolayer, has arrested a great interest for electronic devices due to its predicted ultra-high carrier mobility (>1.8×10^4 $cm^2\cdot V^{-1}\cdot s^{-1}$) [25]. For a relatively short period, decent progresses have been made on both experiment [25], [26] and theory [27], [31], [50]. Even at its early stage, a reasonably high field-effect mobility (~150 $cm^2\cdot V^{-1}\cdot s^{-1}$) and a large ON/OFF current ratio (>10^5) have been reported for GeH field-effect transistors (FETs) [26]. Quantum transport simulations have also predicted that short-channel GeH FETs would be promising for high-performance device applications due to its large injection velocity [39]. Moreover, the performance of GeH FET has been evaluated for complementary metal-oxide-semiconductor (CMOS) technology, exhibiting the superior performance of GeH FETs over other similar 2D material devices for electronic circuits in terms of energy-delay product [38]. However, ohmic contacts were assumed in the previous studies [31], [38], [39], and the possible performance degradation due to Schottky contacts in GeH FET has not been studied. Therefore, detailed understanding of GeH Schottky barrier (SB) FET (SBFET) is currently missing from the field although practical nanoelectronic devices are generally made with metal contacts.

In this chapter, we investigate the performance variation of GeH FETs using different Schottky contacts through self-consistent atomistic quantum transport simulations. First, we will perform a comparative study for two ohmic-contact GeH FETs using different device structures: one with doped source/drain (so-called MOSFET) and the other with metal contacts (SBFET). Next, we will compare GeH SBFET with BP SBFET to discuss the effect of different channel materials using the same device structure. Then, we will investigate the performance of GeH SBFETs by varying SB heights at the source and the drain. Finally, we will optimize the intrinsic performance of GeH SBFET by engineering Schottky barrier along with the threshold voltage. We will also benchmark GeH SBFET against GeH and BP MOSFETs in a perspective of energy-delay product.

5.2 Simulation Setup

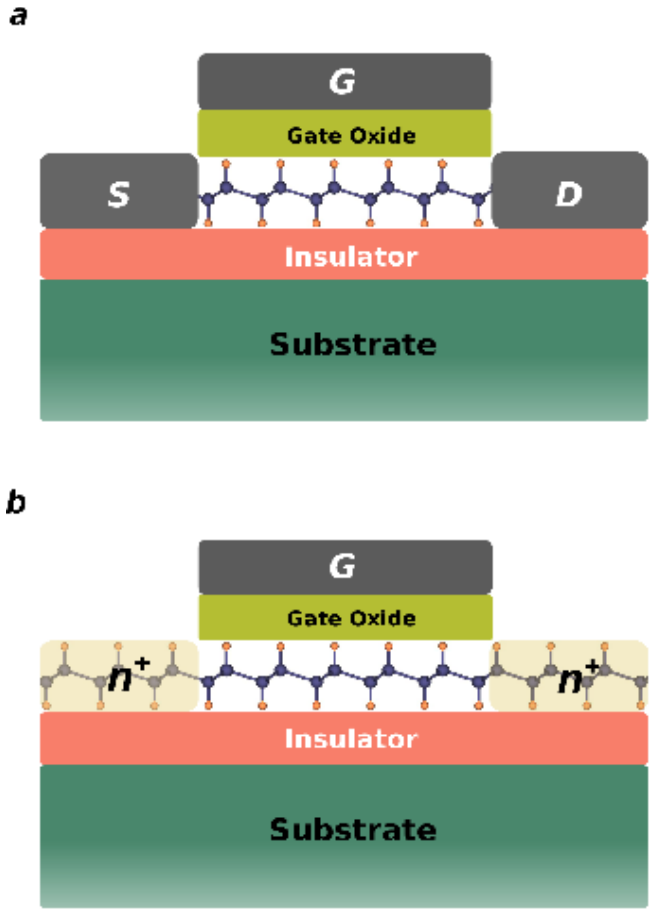

Figure 5.1 ***Simulated device structure*****. Germanane (GeH) field-effect transistor (FET) with (a) metal contacts (SBFET) and (b) n-doped source/drain (MOSFET).** [51]

Schematics of the device structures for GeH FETs used for our simulations are plotted in Figure 5.1, in which monolayer GeH (bandgap of E_g = 1.56 eV) is employed for the channel material. The following device parameters are used for the nominal devices: 14-nm channel length (L_{ch}); 2.75-nm-thick HfO_2 ($\kappa = 25$) gate dielectric (equivalent oxide thickness of EOT = 0.43 nm). For the SBFET (Figure 5.1(a)), the SB height (Φ_{Bn}) of 0.22 eV is used for the nominal device based on a recent experiment [52]. For the GeH MOSFET (Figure 5.1(b)), 20-nm source and drain extensions are *n*-doped with a doping concentration of 5.5×10^{12} cm^{-2}. Device parameters such as channel length and SB height will be varied to explore their impacts on the device performance.

Electronic properties of GeH are described by tight-binding parameters, which have been achieved through numerical fitting of the density functional theory band structure [39]. For atomistic quantum

transport simulations, the non-equilibrium Green's function (NEGF) method is employed [35], and the self-consistent charge density and electrostatic potential are achieved by solving the Poisson's equation alongside the transport equation. Current and charge density are calculated using the converged electrostatic potential energy. The open boundary conditions brought by the source and the drain are treated differently for the two distinct devices through self-energies ($\Sigma_{S,D}$). For a MOSFET, the self-energy is calculated by $\Sigma_{S,D} = \tau g_s \tau^{\dagger}$ (τ is a coupling matrix between the adjacent unit cells; g_s is the surface Green's function), in which g_s is calculated in an iterative manner. On the other hand, for a SBFET, self-energies are treated phenomenologically to mimic the continuous carrier injection from the metal to the channel, and the values are given by $-it_0$ [53]. In this study, we have used a nominal value of t_0 = 1.3 eV, which can provide a reasonable value for the imaginary part of the self-energy considering broadening, for both GeH and BP for a fair comparison of different channel materials. It is known that a variation in t_0 does not affect the qualitative result [53], and therefore, a different value of t_0 will not change the conclusion of this study. Ballistic transport is assumed due to the short channel length considered in this study. In principle, scattering can degrade the performance of FETs particularly for long-channel devices, however its impact will be limited for the size of devices we consider here.

5.3 Comparison of GeH SBFET and MOSFET

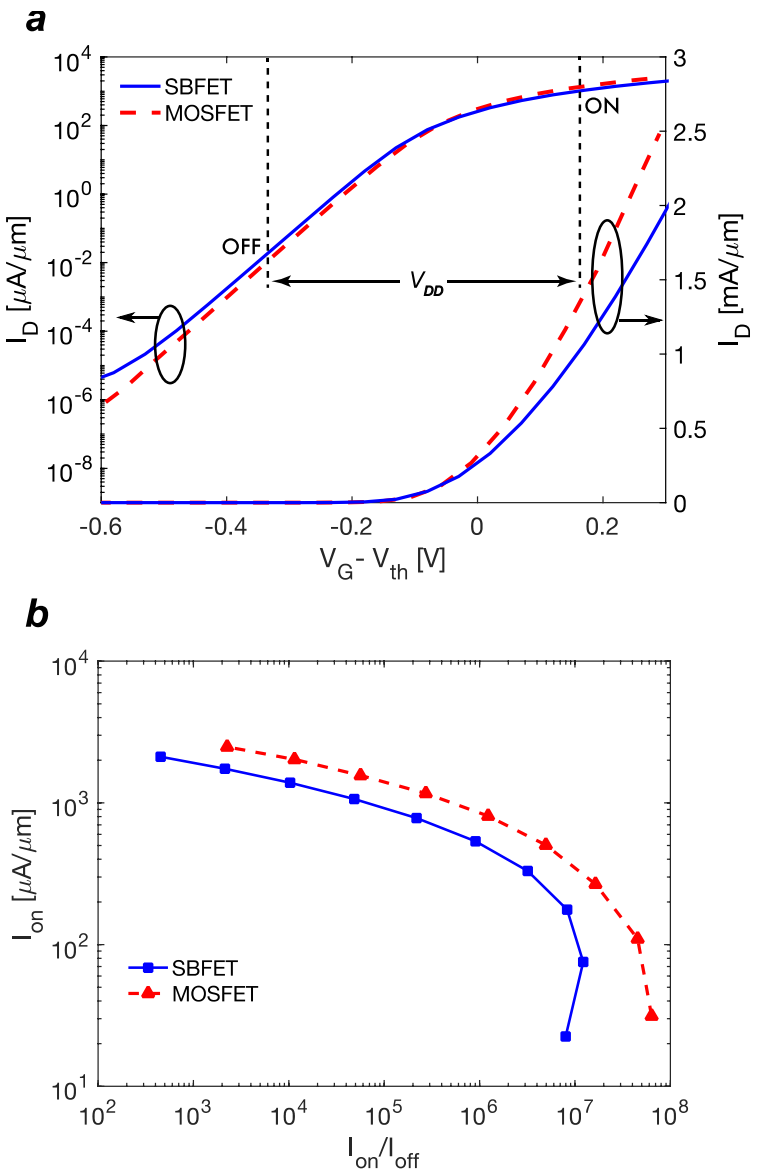

Figure 5.2 ***Transfer characteristics of GeH FETs with Ohmic contacts.*** **(a)** I_D **vs.** $(V_G–V_{th})$ **characteristics for the GeH FETs with zero SB height (Φ_{Bn} = 0 eV) metal contacts (SBFET) and doped source/drain (MOSFET) at** V_D **= 0.5 V on a logarithmic scale (left axis) and on a linear scale (right axis). (b)** I_{on} **vs.** I_{on}/I_{off} **for the same devices.** [51]

First, we compare the transfer characteristics of ohmic-contact GeH FETs using two different device structures: one with zero SB height (Φ_{Bn} = 0 eV) metal contacts (SBFET) and the other with doped source/drain (MOSFET). Figure 5.2(a) exhibits I_D vs. $(V_G–V_{th})$ of the two, and both devices show

excellent switching characteristics with small subthreshold swing (SS ~63 mV/dec). However, the SBFET with Φ_{Bn} = 0 eV shows lower on current compared to the MOSFET by 20%. To understand this, we have plotted energy-resolved current spectrum along with the conduction band (E_c) profile at the on state ($V_G - V_{th}$ = 0.25 V) in Figure 5.3. In case of SBFET, current consists of two components: thermionic current ($0 \leqslant E \leqslant 0.15$ eV) and tunneling current (-0.25 eV $\leqslant E < 0$ eV) as it can be seen in Figure 5.3(a). Although SB height is zero at the source-channel interface, a significant number of injected carriers can still be hampered by the tunneling barrier, resulting in suppressed transmission and hence lower on current with the SBFET structure. On the other hand, for the MOSFET, the majority of current flows over the channel potential without facing the tunnel barrier, as shown in Figure 5.3(b), and therefore, the on current of the MOSFET is larger than that of SBFET.

In addition, MOSFET also shows better OFF-state characteristics with lower leakage current. To explain this, we have plotted the energy-resolved current spectrum in the OFF state ($V_G - V_{th} = -0.55$ V) in Figure 5.4. It is observed in Figure 5.4(a) that tunneling can be a significant leakage path for the SBFET, whereas this is not the case of MOSFET as shown in Figure 5.4(b). It should be noted that, although the same 14-nm channel is used for both devices, the SBFET exhibits a relatively shorter tunneling width (13 nm) compared to that of the MOSFET (17 nm) at E = 0 eV.

To assess both on and OFF states comprehensively, we have plotted I_{ON} vs. I_{ON}/I_{OFF} in Figure 5.2(b) for GeH SBFET and MOSFET by shifting the operation voltage window at V_{DD} = 0.5 V (shown in Figure 5.2(a)). on current and OFF current are obtained by reading the current value at the edges of the V_{DD} window [37]. For the on current requirement of 500 μA/μm, SBFET can have $I_{ON}/I_{OFF} = 9\times10^5$, demonstrating promising switching characteristics of GeH SBFET, although the overall performance of the device can be limited by the metal-semiconductor (M-S) junction compared to the MOSFET structure. For five orders of magnitude in I_{ON}/I_{OFF}, the on current of SBFET can be as large as ~1 mA/μm.

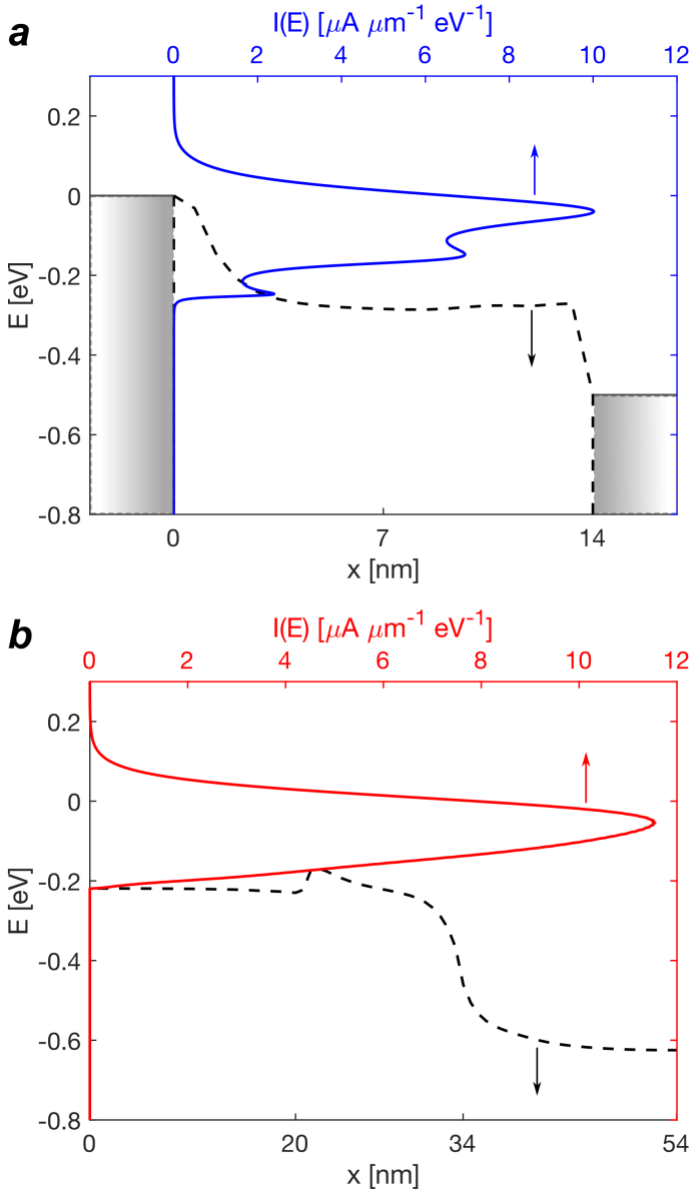

Figure 5.3 Energy-resolved current spectrum of (a) GeH SBFET (blue solid line; top axis) and (b) GeH MOSFET (red solid line; top axis) in the on state (V_G–V_{th} = 0.25 V). Conduction band (E_C) profiles (dashed lines; bottom axis) are also shown for both devices. [51]

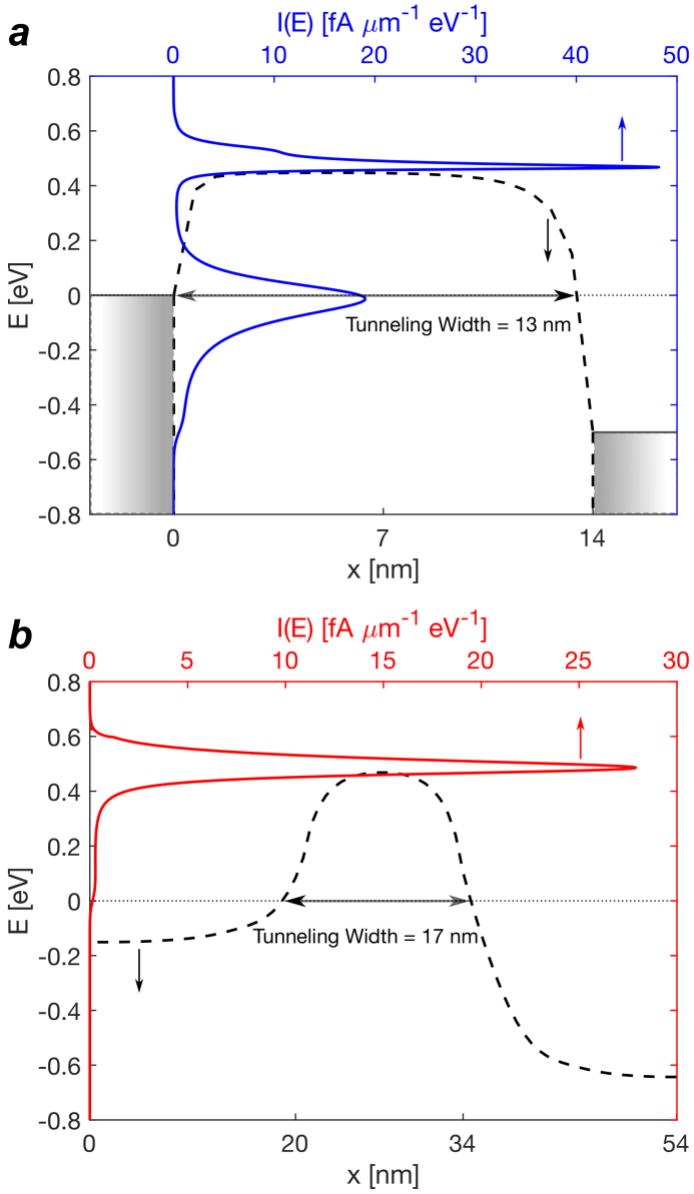

Figure 5.4 Energy-resolved current spectrum of (a) GeH SBFET (blue solid line; top axis) and (b) GeH MOSFET (red solid line; top axis) in the OFF state (V_G–V_{th} = -0.55 V). Conduction band (E_C) profiles (dashed lines; bottom axis) are also shown for both devices. [51]

5.4 Comparison of GeH SBFET and BP SBFET

A recent experimental work on a germanane Schottky diode has shown that the SB height at the M-S junction was estimated to be 0.22 eV [52]. Therefore, in this section, we will use Φ_{Bn} = 0.22 eV for the

SB height of the nominal SBFET. For a comparative study, monolayer BP has been adopted, which has a similar band gap (E_g = 1.52 eV) as GeH but a relatively large effective mass (anisotropic effective mass of 0.17m_0 and 0.87m_0 for electrons) and larger density of states (DOS).

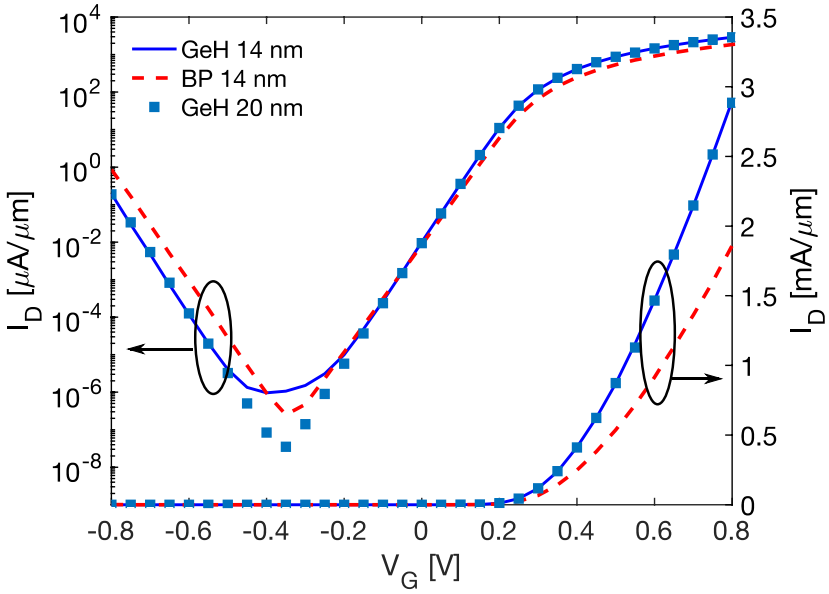

Figure 5.5 I_D–V_G characteristics of 14-nm GeH SBFET (blue solid line), 14-nm BP SBFET (red dashed line), and 20-nm GeH SBFET (blue square marker). The Schottky barrier height of Φ_{Bn} = 0.22 eV is used for all three devices. The plots are shown on a logarithmic scale (left axis) and on a linear scale (right axis). [51]

Figure 5.5 shows the ambipolar I_D–V_G characteristics of 14-nm-channel GeH SBFET (blue solid lines) and BP SBFET (red dashed lines) at V_D = 0.5 V. Both devices exhibit excellent switching characteristics with steep subthreshold slope (SS ~64 mV/dec), while GeH SBFET shows larger on current (I_{ON} ~3 mA/μm at V_G = 0.8 V) than BP SBFET by 45%. In Figure 5.6(a), the potential profiles of the GeH and BP FETs are plotted in the on state (V_G = 0.75 V). Although GeH SBFET has a slightly lower potential barrier compared to BP SBFET due to its lower DOS and hence the ease of potential modulation by the gate [38], the difference between the two is minimal. Therefore, we modeled the M-S junction by creating a simplified triangular Schottky barrier, as shown in the inset of Figure 5.6(a), for both materials to compare the transport properties by excluding the minor difference in the self-consistent potential. Notably, in this test, we have used a single M-S junction only at the source-channel interface to fully focus on the transport property through the junction on the source side. Another

junction at the drain, which has a relatively minor effect, is replaced by a semi-infinite lead for a reflectionless contact. This approximation is valid for our nominal device at the on state since the potential profile becomes almost flat near the drain, as shown in the main panel of Figure 5.6(a), due to the relatively small SB height. The simulated energy-resolved current spectrums in Figure 5.6(b) indicate that current through the same triangular tunnel barrier can be significantly larger with GeH rather than with BP since the tunnel barrier looks more transparent for electrons in GeH due to its smaller effective mass. In addition, the relatively insignificant charging effect and lower potential in GeH FET can also provide a larger energy window for carrier injection, leading to further increase in current.

The OFF-state characteristics of 14-nm-channel GeH and BP SBFETs are depicted in Figure 5.7(a) and (b), respectively. It is observed that GeH has significant source-to-drain tunneling current, which is not the case of BP SBFET. This explains the larger minimum leakage current (I_{min}) of GeH FET, compared to that of BP FET, for the same channel length (Figure 5.5). However, if a longer channel is used, the leakage current in GeH FET can be suppressed, which is proven in Figure 5.7(c) at L_{ch} = 20 nm, in which I_{min} is reduced by ~2 orders of magnitude compared to that of the 14-nm-channel device (Figure 5.5).

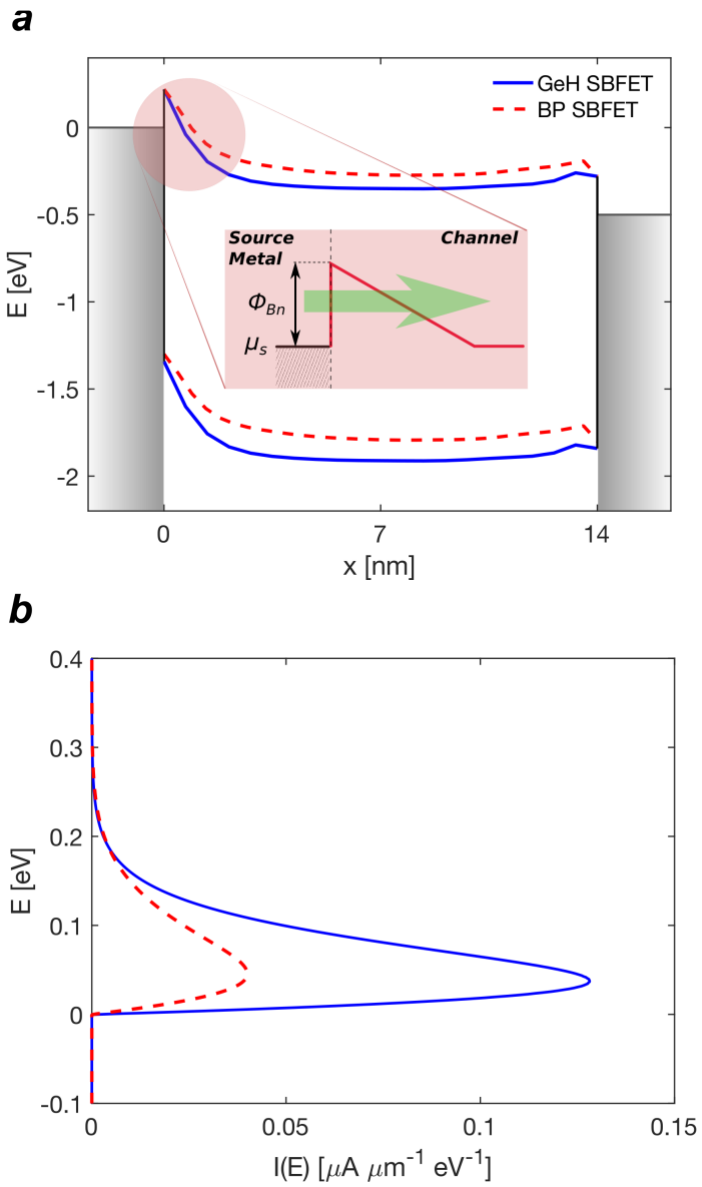

Figure 5.6 Conduction band (E_C) and valence band (E_V) profiles along the devices for GeH (blue solid line) and BP (red dashed line) SBFETs at V_G = 0.75 V. (Inset) The Schottky contact at the metal-semiconductor (M-S) junction is modeled by a triangular potential barrier. (b) Energy-resolved current spectrum for the M-S junction with GeH (blue solid line) and BP (red dashed line). [51]

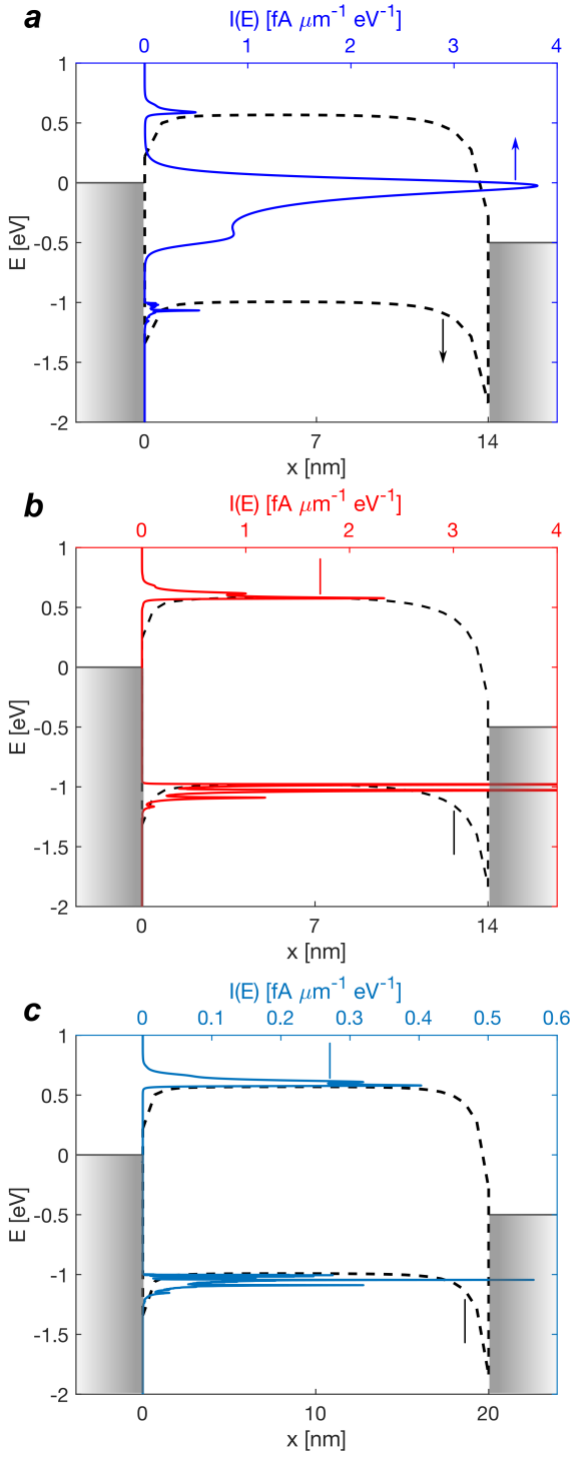

Figure 5.7 Energy-resolved current spectrum (solid lines) and energy band profiles (dashed lines) along the devices for (a) 14-nm GeH SBFET, (b) 14-nm BP SBFET, and (c) 20-nm GeH SBFET, at V_G = -0.35 V where minimum leakage currents are achieved. [51]

5.5 Effect of Schottky Barrier Height

The effects of the Schottky barrier height on the transfer characteristics are studied in this section. First, we investigate the on-state performance of GeH SBFET by ploting the I_D vs. (V_G–V_{th}) characteristics for different SB heights of 0, 1/8 E_g, 1/4 E_g, 3/8 E_g, and 1/2 E_g (where E_g is 1.56 eV) in Figure 5.8. It shows a monotonic decrease of on current with increasing SB heights. The zero-SB-height device exhibits ~150% larger I_{ON} than the one with $\Phi_{Bn} = E_g/2$. This is attributed to the fact that electrons in the larger SB device should overcome greater tunnel barriers at the M-S junctions as shown in Figure 5.9, where

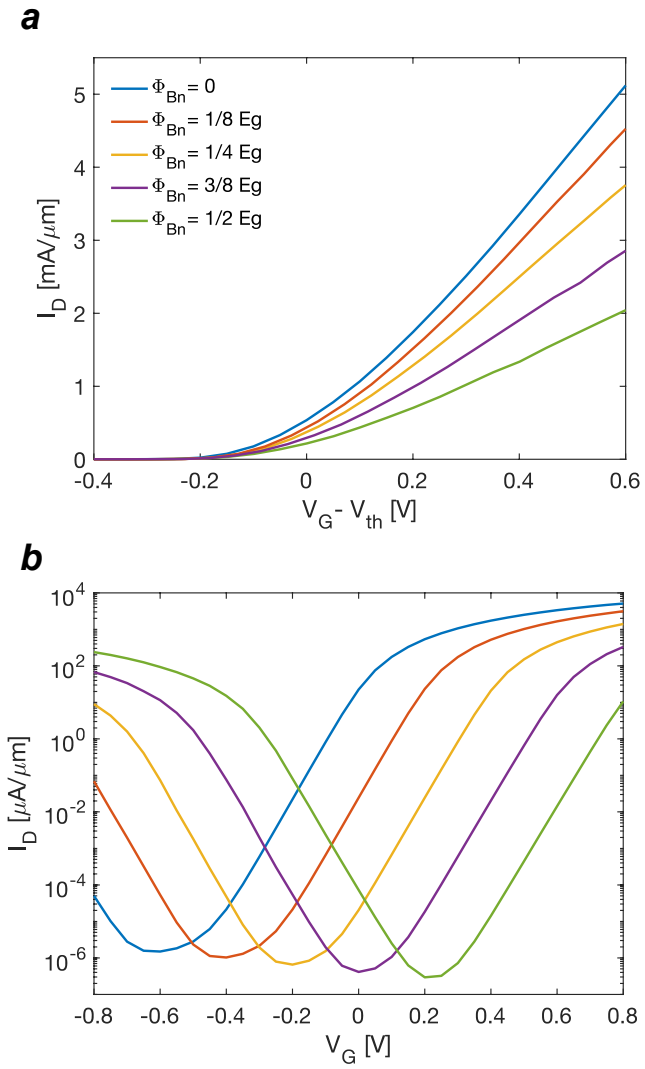

Figure 5.8 Transfer characteristics of GeH SBFETs with different SB heights of 0, 1/8 E_g, 1/4 E_g, 3/8 E_g, and 1/2 E_g at V_D = 0.5 V. (a) I_D vs. (V_G–V_{th}) characteristics on a linear scale, considering

the threshold voltage (V_{th}) shift. (b) I_D–V_G curves on a logarithmic scale, in which the same colors are used for different SB heights as in (a). [51]

the energy-resolved current spectrums and the channel potential energies for Φ_{Bn} = 0 eV and $E_g/2$ are depicted at V_G–V_{th} = 0.5 V. As the SB height increases, the tunneling becomes dominant and the contribution of thermionic current is gradually reduced.

In Figure 5.8(b), we also plotted the logarithmic-scale I_D–V_G characteristics of GeH SBFET for the different SB heights. While all devices commonly exhibit the ambipolar behavior of SBFETs with the V_{th} shifts, it is observed that the minimum leakage current exponentially decreases with the increase of SB height, as shown in Figure 5.10(a). To understand this, we have plotted the potential energy profile along the channel at the gate voltage providing the minimum leakage current for Φ_{Bn} = 0 eV and $E_g/2$ in Figure 5.10(b). It should be noted that the effective tunneling barrier becomes shorter than the actual channel length (14 nm) with Φ_{Bn} = 0 eV, whereas this is not the case with $\Phi_{Bn} = E_g/2$. Therefore, the direct source-to-drain leakage current can be significantly larger with Φ_{Bn} = 0 eV as shown in Figure 5.10(c).

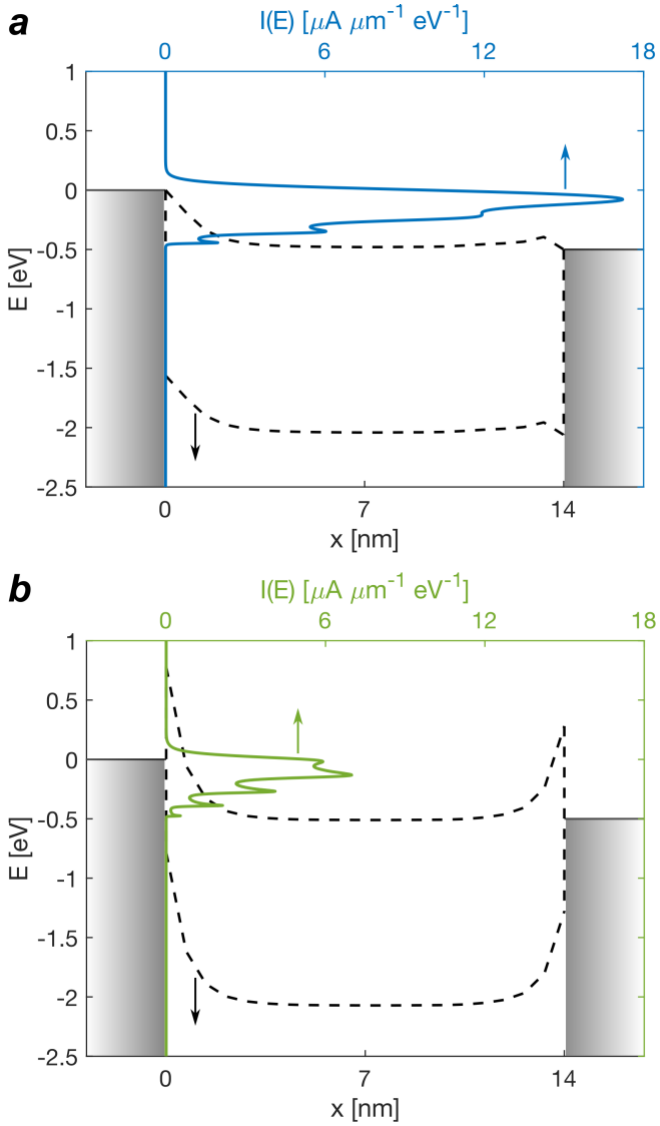

Figure 5.9 The current spectrum, $I(E)$ (solid lines; top axis) in the on state ($V_G - V_{th}$ = 0.5 V) for (a) Φ_{Bn} = 0 eV and (b) Φ_{Bn} = 1/2 E_g. E_C and E_V (dashed lines; bottom axis) are also shown along the channel. [51]

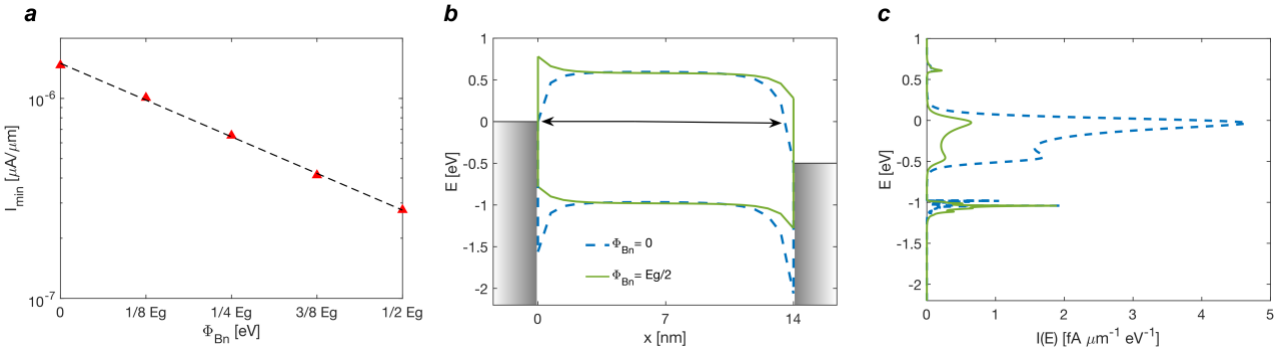

Figure 5.10 (a) Minimum leakage current, I_{min} for different SB heights. (b) E_C and E_V profile along the channel for the devices with Φ_{Bn} = 0 eV and 1/2 E_g at the gate voltages providing the minimum leakage current for each device. The black arrow indicates the tunneling width for carriers at $E \approx 0$ eV. (c) Energy-resolved current spectrum, $I(E)$ corresponding to the potential shown in (b), in which the same colors are used for different SB heights as in (b). [51]

5.6 Intrinsic Device Performance

Finally, we assess the intrinsic performance of GeH SBFET. Here we evaluate intrinsic delay (Figure 5.11(a)) for the limitation of device switching speed and power-delay product (Figure 5.11(b)) for the dynamic power dissipation per switching [54], by varying the SB height from 0 eV to $E_g/2$. It is observed that switching speed monotonically increases (*i.e.*, the delay decreases) as the device operational region is shifted from the sub-threshold to the super-threshold region for all devices with different SB heights, while the switching energy monotonically increases with the same shift. Two different values of τ and PDP can be observed at large I_{ON}/I_{OFF} (*i.e.*, low gate voltages) due to the leakage current explained above, and the same behavior was also reported earlier for GeH MOSFETs [38]. In Figure 5.11(c), we have plotted τ (right axis) and PDP (left axis) as a function of SB height for fixed $I_{ON}/I_{OFF} = 10^4$ and 10^5. In general, for a given I_{on}/I_{off}, GeH SBFET with a larger SB height exhibits larger delay (slower switching speed) but lower energy dissipation per switching. At $I_{ON}/I_{OFF} = 10^5$, intrinsic delay is ~45 fs with $\Phi_{Bn} \leq E_g/4$, but shows a significant increase beyond 3/8 E_g, resulting in 73 fs with $\Phi_{Bn} = E_g/2$. In comparison, PDP decreases linearly with increasing SB height and shows 22 aJ/µm and 12 aJ/µm at $\Phi_{Bn} = 0$ eV and $E_g/2$, respectively, at $I_{on}/I_{off} = 10^5$. On the other hand, for a fixed Φ_{Bn}, it is observed that the delay is reduced, and PDP is increased for a smaller I_{ON}/I_{OFF}.

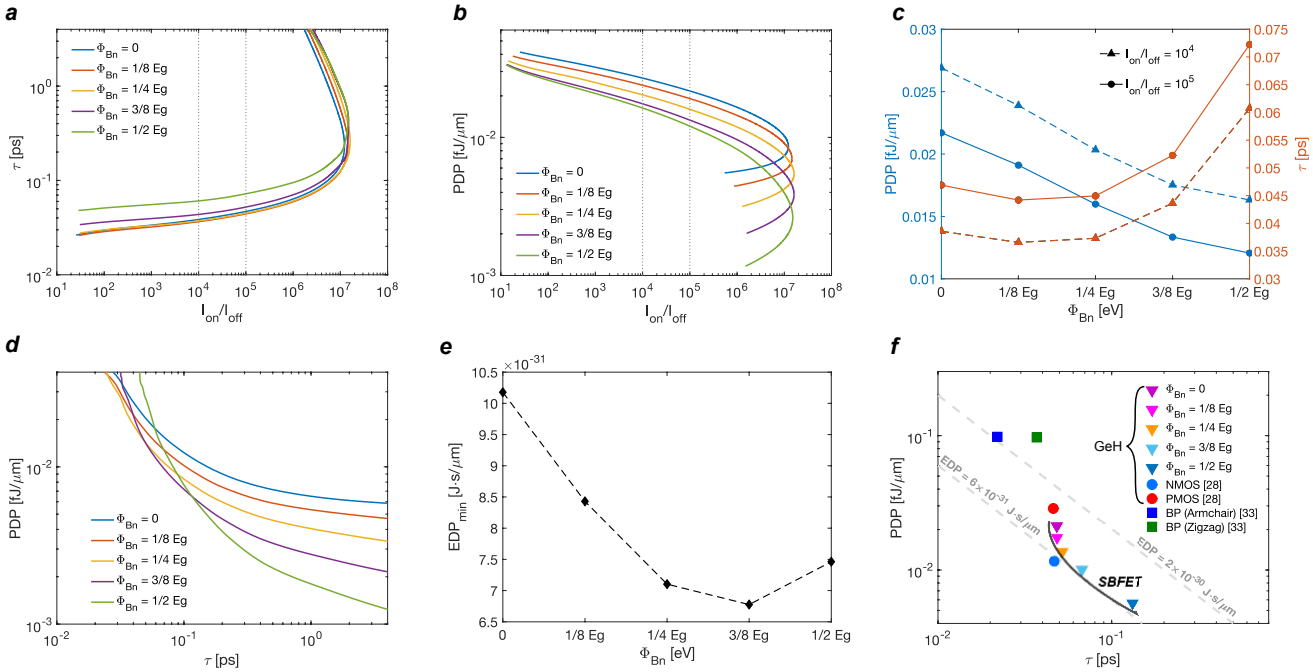

Figure 5.11 ***Intrinsic device performance with different SB heights.*** **(a) Intrinsic delay (τ) and (b) power-delay product (PDP) vs. I_{on}/I_{off}. (c) PDP (blue lines; left axis) and intrinsic delay (orange lines; right axis) as a function of Φ_{Bn} for the I_{on}/I_{off} of 10^4 (triangles) and 10^5 (circles) (See the dotted lines in (a) and (b)). (d) PDP vs. intrinsic delay with different SB heights. (e) Minimum energy-delay product (EDP) for different Φ_{Bn}. (f) EDP of GeH SBFET, GeH MOSFET and BP MOSFET shown on the PDP-delay plot for benchmarking.** [51]

The inverse relation of PDP and τ is plotted in Figure 5.11(d), which indicates the trade-off between the operation frequency and the energy cost. Using this plot, the minimum energy-delay product (EDP = PDP·τ) can be found for each Φ_{Bn}, which has been plotted in Figure 5.11(e). It shows that the global minimum of EDP is observed near Φ_{Bn} = 3/8 E_g (0.59 eV), indicating that the optimal EDP should be determined by considering SB height as well as device speed and energy dissipation. The minimum EDP found for different Φ_{Bn} has been plotted on the PDP-delay plan in Figure 5.11(f), where GeH SBFETs are benchmarked against other similar devices such as GeH MOSFETs [38] and BP MOSFETs [46]. The gray dashed lines in Figure 5.11(f) are shown for equi-EDP values. It is observed that, in general, GeH FETs have less EDP than BP FETs. Among the GeH devices, GeH NMOS exhibits the lowest EDP of ~6×10^{-31} J·s/μm. EDP of GeH SBFETs asymptotically approach the NMOS value as Φ_{Bn} increases, forming a curve shown in Figure 5.11(f), and GeH SBFET with Φ_{Bn} = 3/8 E_g shows the

closest EDP of 6.8×10^{-31} J·s/μm. This demonstrates that GeH SBFET can have as promising performance as GeH MOSFET in terms of EDP through careful engineering of Schottky contact.

5.7 Summary

By using atomistic quantum transport device simulations based on the non-equilibrium Green's function method, we have investigated transfer characteristics of GeH Schottky barrier FETs considering different barrier heights. In particular, we have studied the impact of SB height on the intrinsic device performance, such as delay and power-delay product, to find the optimal operation region and the SB height for minimum energy-delay product. Moreover, we have also simulated GeH MOSFET and BP SBFET to develop in-depth understanding of metal contacts (against doped source/drain) in GeH FETs, and the benefit/drawback of GeH (as compared to BP) as a channel material of FET. Our simulation results and the comprehensive assessment on the material and the device structure, not only reveal the great potential of GeH FETs for practical device applications, but also give useful insight into device-level optimization through Schottky barrier engineering. The main results of this study can be summarized as follows.

1) Even with zero barrier height, ohmic-contact GeH SBFET suffers from the performance degradation in the on state, compared to the GeH MOSFET counterpart with doped source/drain, by ~20% due to the existing tunnel barrier.

2) Despite relatively lower density of states, GeH SBFET shows superior on-state characteristics than BP SBFET. This is attributed to the fact that the injection of carriers at the source-channel junction is critical for the performance of short-channel devices in the ballistic regime, and the electrons in GeH with smaller effective mass can be more favorable to tunneling for higher current.

3) Although the flow of carriers in GeH SBFET can be limited by the inherent barrier at the M-S junction, as compared to that in GeH MOSFET, the energy-delay product of SBFET can be as comparable as that of MOSFET through elaborate engineering of operation voltages and Schottky barrier. In general, with increasing the SB height, GeH FET exhibits slower switching speed but lower energy dissipation, indicating the trade-off to be considered. Our simulation results show that the global minimum of EDP for GeH SBFET can be obtained with the SB height of ~0.59 eV.

Chapter 6 Conclusion and Future Work

6.1 Conclusions

In this thesis, a novel 2-D material, germanane, and its potential application for nanoelectronics devices are thoroughly investigated from material parameterization to device simulation and finally circuit analysis. First, the performance limit of monolayer GeH FETs was discussed. Our results showed that GeH FETs exhibit high I_{ON} (>2 mA/μm) and large g_m (~7 mS/μm) as well as excellent switching characteristics (SS ~64 mV/dec), due to the very light effective mass of GeH. Our scaling study revealed that ~14 nm will still be suitable for the channel length of GeH FET as it may suffer from significant short channel effects if the channel length becomes less than 10 nm. We have also benchmarked GeH FET against MoS_2 device, which suggested that GeH has clear benefits for high-performance device applications over MoS_2.

The next stage of the work focused on the potential application of GeH FETs for CMOS technology. We first investigated both device performance of n-type and p-type GeH MOSFETs where n-type GeH exhibits ~40% better ON-state performance due to the higher carrier velocity of electrons. We showed a clear advantage of GeH over MoS_2 and BP in terms of energy-delay product by calculating the intrinsic device metrics (intrinsic delay and power delay product). In the analysis of GeH-based digital circuit (CMOS inverter chain), we located the optimal operating condition of GeH FETs to minimize energy-delay product by engineering V_{DD} and threshold voltage. Our comprehensive study including material, device and circuit optimization suggests that germanane can be a significant contender for electronic devices of next-generation CMOS technology.

Finally, GeH Schottky barrier FETs with metal contact have been investigated. In particular, we have studied the impact of SB height on the intrinsic device performance, exhibiting that the GeH SBFET suffers from ~20% performance degradation compared to MOSFET counterpart even with zero barrier height. Despite the limitation in on-state performance of GeH SBFET, the energy-delay product of it can be comparable as that of MOSFET through carefully engineering of operating region and contact property. Moreover, by benchmarking with another similar 2-D materials (black phosphorus MoS_2), GeH SBFET showed superior on-state device performance than does BP SBFET, because of the smaller effective mass of GeH which can be more favorable to tunneling.

In this thesis, we have provided fresh insights into germanane FETs through comprehensive study including materials parametrization, device simulation and circuit analysis, which could also be extended to the engineering practice of other similar 2D semiconductor FETs.

6.2 Future Work

6.2.1 Multi-layer GeH

So far, our discussion has only focused on monolayer GeH FETs and we have not discussed multi-layer GeH FETs. Investigating of multilayer GeH could provide a comprehensive picture of GeH FETs, particularly understanding of the interlayer transport in layered materials. By investigating the multilayer GeH, we may figure out the layer number dependency of its electrical property, such as bandgap or carrier mobility, which may provide a great opportunity to further optimize the device performance of GeH FETs.

6.2.2 Ge-GeH Lateral Heterostructure

Germanene (Ge), single-layered germanium atoms, exhibits extremely high electron mobility. And it has been proven that GeH is promising for nanoelectronics among the available 2-D materials. From an engineering point of view, we may develop the GeH-based device with special properties by considering a device based on lateral heterostructures of metallic Ge and semiconducting GeH. Fabrication of van der Waals heterostructures of germanene and germanane has already been reported. We may theoretically investigate the potential of lateral Ge-GeH heterostructure to fabricate field effect transistor at nanoscale for digital applications. We may adopt a first-principle approach: (1) DFT simulation to understand the electronic property of Ge-GeH heterostructure; (2) the extraction of tight-binding parameters based on localized Wannier functions.

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